WaveArtist™ 010 Audio System Device

Designer's Guide (Preliminary)

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WaveArtist™ 010 Audio System Device Designer's Guide

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1. INTRODUCTION

1.1 Summary

The Rockwell WaveArtist™ 010 (RWA010) and WaveArtist™ 030 (RWA030) are audio system devices in small, low profile, PQFP/TQFP packages. These devices provide increasing functionality from FM synthesis (RWA010), to FM and high quality music wavetable synthesis (RWA010 and RWA030), to FM and high quality music wavetable synthesis with optional effects processor upgrade (RWA010, RWA030, and RWA035). (See Table 1-1.)

The RWA010 Audio System Controller and Codec supports FM synthesis, 16-bit stereo audio with simultaneous record and playback, and ISA bus Plug-and-Play (PnP) interface with 16-bit (RWA010) or 12-bit (RWA011) address for cost effective, expandable audio and audio/modem system designs. The RWA010 is also compatible with DOS applications that use Sound Blaster Pro, Yamaha OPL3, AdLib, and MPU-401 interfaces. Also supported is a game port with internal timers, and for the RWA011 only, an enhanced IDE CD-ROM interface. General MIDI compatible wavetable synthesis is provided by adding the RWA030 Music Processor (Figure 1-1). Unless otherwise noted, all references to the RWA010 also include the RWA011. The RWA010 is packaged in a 144-pin TQFP. This document describes the RWA010 and RWA011.

The RWA010, when used with a Rockwell modem, provides seamless integration of high speed data/fax modem, voice/audio, AudioSpan simultaneous voice and data, and speakerphone functions.

The RWA030 Music Processor, featuring Audio by Kurzweil and special audio effects, in an 80-pin PQFP, supports high quality sound designs in either RWA010 or external DAC interface configuration. It connects to the RWA010 or other controller, a 2MB or 1MB wavetable ROM, and an optional downloadable sound sample DRAM (up to 8MB), and the optional RWA035. The RWA030 and RWA035 are described in the RWA030 Music Processor Designer's Guide (Order No. 1103).

The RWA035 Effects Processor Upgrade, in an 80-pin PQFP, adds professional quality sound processing such as concert hall and other spatial features to the RWA030. The RWA035 connects to an external DRAM.

Host software, compatible with the Windows Sound System (WSS), is provided for Windows 95, Windows 3.1x, Windows NT, and DirectSound environments. A software utility is also available to configure the PnP interface in an MS-DOS environment.

FCC part 15 and part 68 approved reference hardware designs are available.

1.2 Features

- RWA010 Audio System Controller and Codec
  - 16-bit stereo audio in a single mixed-signal device
        16-bit delta sigma codec with >80 dB SNR
        Sound Blaster Pro compatible
        Simultaneous (full-duplex) record and playback
        8-bit and 16-bit PCM sample record and playback from 4 kHz to 44.1 kHz
        Digital sample rate conversion with 0.7 Hz resolution
        Integrated OPL3/OPL2 and AdLib compatible FM synthesis with no external DAC required
        5 external analog input channels (4 stereo, 1 mono)
        Independent left and right channel mixers each with 5 external inputs and 1 internal input (digitally summed FM, optional wavetable, and PCM signals)
        2 external analog output channels (1 stereo, 1 mono)
        Uses single crystal oscillator
  - Integrated hardware interfaces
        MPU-401 MIDI UART compatible
        Enhanced IDE CD-ROM compatible (RWA011)
        Joystick with internal timers (game port compatible)
        ISA bus PnP interface
  - Programmable PnP resource data
- RWA030 Music Processor in 80-pin PQFP
  - General MIDI compatible wavetable synthesis supports 32 voices at 44.1 KHz
  - Basic effects for reverb, chorus, and 3D spatialization
  - Treble and bass equalization
  - Interface to 2MB or 1MB wavetable ROM
  - Interface to sound sample DRAM (up to 8MB)
  - Interface to RWA035 Effects Processor Upgrade
- RWA035 Effects Processor Upgrade in 80-pin PQFP
  - Full effects for reverb, chorus and delay
  - Spatial placement effects
  - Interface to DRAM (up to 512 kB)
- Low profile, small footprint packages
  - RWA010: 144-pin TQFP
  - RWA030: 80-pin PQFP
- Power management
- Applications
  - Integrated audio/telephony cards
  - Motherboards, notebooks, add-on cards
  - PC audio/games
  - Windows Sound System (WSS) and DirectSound

Table 1-1. Models and Functions

Functions	Required Devices		
	RWA010/RWA011 (Note 1)	RWA010/RWA011 (Note 1), RWA030, and RWA031/RWA032 ROM (Note 2)	RWA010/RWA011 (Note 1), RWA030, RWA031/RWA032 ROM (Note 2), and RWA035
FM Synthesis	X	X	X
High Quality Wavetable Synthesis 3D Spatialization Effects (Reverb and Chorus) Equalization (Treble and Bass)	—	X	X
Professional Quality Effects Processing (Reverb, Chorus, Delay, Concert, Auditorium, etc.)	—	—	X
Notes: RWA010 supports 16-bit PnP address but not CD-ROM interface; RWA011 supports 12-bit PnP address and CD-ROM interface. RWA031/RWA032 is the optional 1MB/2MB wavetable ROM for the RWA030.			

CONTROL,
ADDRESS,
DATA

ROCKWELL
MODEM
(e.g., RC366ACF/SP)

TELEPHONE
LINE
INTERFACE

TELEPHONE LINE

TYPICAL
MODEM
CONNECTION

CONTROL

DATA

RWA011 ONLY

ENHANCED
IDE
CD-ROM
INTERFACE

CD-ROM

CD-ROM SIGNALS

ISA
BUS

CONTROL,
ADDRESS,
DATA

RWA010/RWA011
AUDIO
SYSTEM
CONTROLLER
AND
CODEC
[144-PIN TQFP]

MONOIN
MONOOUT
MICROPHONE (LMIC, RMIC)
LINE IN (LLINE, RLINE)
LINEOUT (LOUT, ROUT)
AUX IN 1 (LAUX1, RAUX1)
AUX IN 2 (LAUX2, RAUX2)

MIDI AND JOYSTICK SIGNALS

GAME PORT

PNP
EEPROM
(256B)

RWA030
MUSIC
PROCESSOR
[80-PIN PQFP]

WAVETABLE
ROM
2MB OR 1MB

OPTIONAL
DRAM
(UP TO 4M x 16)

RWA035
EFFECTS
PROCESSOR
UPGRADE
[80-PIN PQFP]
[OPTIONAL]
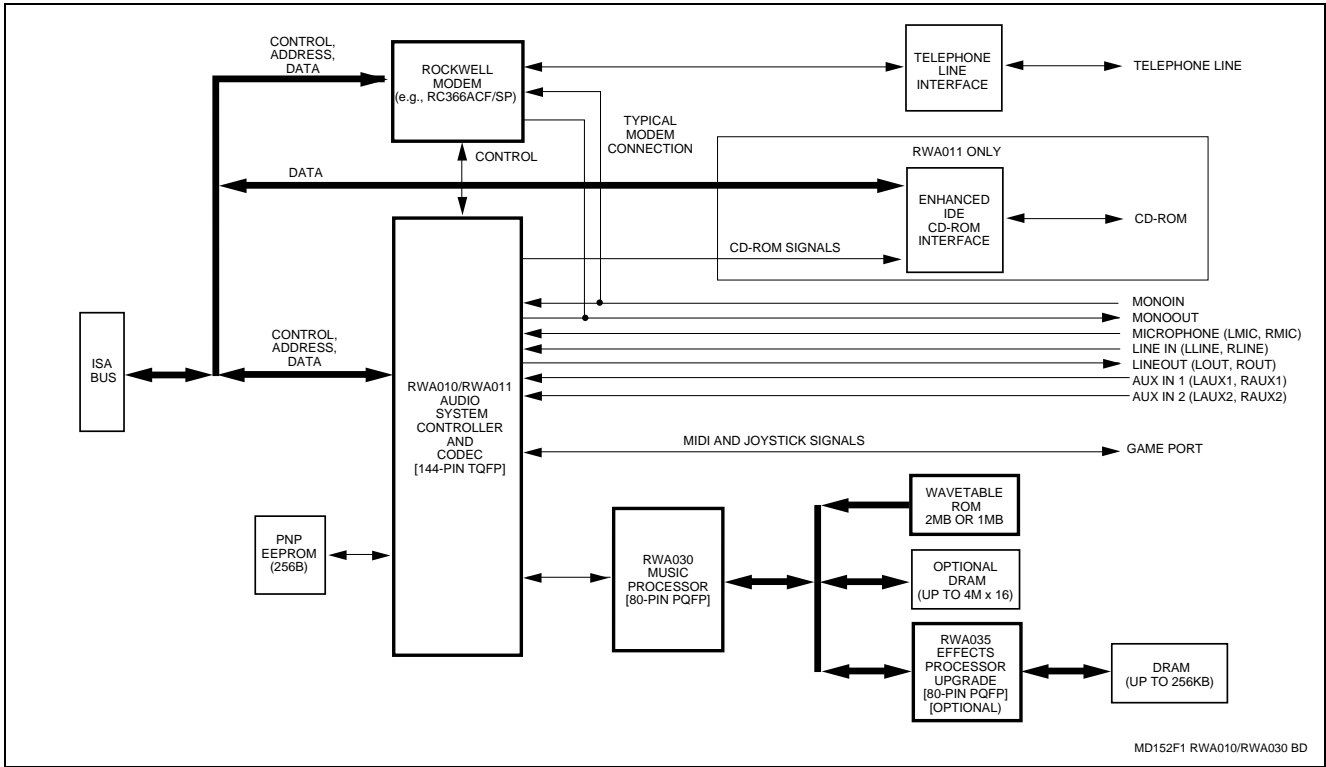
DRAM
(UP TO 256KB)

MD152F1 RWA010/RWA030 BD

Figure 1-1. RWA010 with RWA030 Block Diagram

2. DESCRIPTION

2.1 General

2.1.1 Sample Rate Conversion

Analog inputs and outputs are sampled at 44.1 kHz. The internal sample rate converter converts PCM samples to sample rates ranging from 4 kHz to 44.1 kHz.

The sample rate converter eliminates the need for an external DAC for the FM synthesis. It also allows the use of a single crystal to support all PCM sample rates.

FM Synthesis

The internal OPL3 and OPL2 compatible FM synthesis engine can operate in either 2-operator or 4-operator mode.

Address, data, and status registers are provided for compatibility with the AdLib/Sound Blaster Pro interfaces.

Stereo Codec/Mixer

An integrated 16-bit delta sigma stereo codec simultaneously mixes, records, and plays with high fidelity.

The record multiplexer for the stereo ADC input selects from four external stereo inputs, one external mono input, or the internal mixer. The mixer combines the external inputs into one stereo input for the record multiplexer.

For playback, separate stereo and mono outputs are provided. The PCM samples are digitally mixed with FM and wavetable synthesizer samples, then converted to analog outputs.

Volume controls are provided on all input and output paths.

Host Software

Windows Sound System (WSS) compatible recording and playback of 16-bit and 8-bit PCM audio is supported in Rockwell-provided host driver software which controls the WaveArtist using the WaveArtist command/status registers.

Music Processor (RWA030 Option)

The RWA030 supports 32-voice polyphony General MIDI wavetable synthesis at 44.1 kHz. It provides several basic audio effects, including reverb, chorus, and 3D sound spatialization (reverb and chorus are not available during wavetable synthesis operation). Additionally, treble/bass equalization can be on FM, PCM, and wavetable synthesis signals. An external 2MB or 1MB ROM is used to store the wavetable sounds.

Sound samples can be loaded into optional external DRAM and played back with the internal synthesis engine. This interface also supports multiple hardware static buffers, allowing games written for DirectSound to playback sounds more efficiently and more than one PCM sample to be mixed at the same time.

For additional high quality effects, an interface is provided to the RWA035 Effects Processor Upgrade device. The RWA035 is programmed with additional sound delay processing algorithms such as concert hall and other spatial effects.

2.1.2 Hardware Signal Interfaces

See 0.

2.1.3 Host Software

Host software is provided for Windows 95, Windows 3.1x (WSS), and Windows NT.

For Windows 3.1 and Windows 3.11, a Hardware Installation Module (HIM) assists in the installation of the Ring 3 driver (MIDI/FM I/O, wave I/O, mixer/volume control, wave sample download), and the Ring 0 VxD (virtual device driver for allocation of physical resources).

For Windows 95, a .INF file works in conjunction with Win 95 PnP to install the Ring 3 driver (wave I/O, mixer/volume control, wave sample download), and the Ring 0 VxD (resource management). DirectSound is also supported for Windows 95.

A DOS utility is available to configure the PnP interface for the MS-DOS environment.

2.2 Specifications

The power requirements are listed in Table 2-2.

The recommended operating conditions are listed in Table 2-3.

The absolute maximum ratings are listed in Table 2-3.

Table 2-2. Current and Power Requirements

Model	Current (ID)		Power (PD)		
	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	
RWA010					f_{IN} = 50.8032 MHz
Normal Mode	140	155	700	815	
Power Down Mode	27	30	135	160	
Notes:					
Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.					

Table 2-3. Recommended Operating Conditions

	Rating	Units
Supply Voltage	5 ±5%	V

Table 2-4. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

3. HARDWARE INTERFACE

3.1 Interface Signals, Pin Assignments, and Signal Descriptions

The RWA010 pin interface signals are shown in Figure 3-1.

The RWA010 pin assignments for the 144-pin TQFP are shown in Figure 3-2.

The RWA010 pin signals are described in Table 3-1.

The hardware input/output interface circuit type are described in Table 3-2.

The digital interface signal characteristics are described in Table 3-3.

The analog-to-digital (ADC) interface signal characteristics are described in Table 3-4.

The digital-to-analog (DAC) interface signal characteristics are described in Table 3-5.

| JA1 |
| JA2 |
| JAX |
| JAY |
| JB1 |
| JB2 |
| JBX |
| JBY |
| MIDI_RX |
| MIDI_TX |

GAME PORT (JOYSTICK AND MIDI) INTERFACE

CRYSTAL CIRCUIT

XTLI
XTLO

MIRQ
MSEL#
RESET#

MODEM INTERFACE

CDIRQ
CDDRQ
CDDACK#
CDSEL#
CDSEL0#
CDSEL1#

CD-ROM INTERFACE (RWA011 ONLY)

ISA BUS INTERFACE

SD[15:0]
SA[15:0 or 11:0]*
IOR#
IOW#
AEN
RESET
IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ15
DRQ1
DRQ5
DRQ6
DRQ7
DACK1#
DACK5#
DACK6#
DACK7#
IOCS16#
SBHE#

WaveArtist 010 (RWA010)/ WaveArtist 011 (RWA011)

RLINE
LLINE
RAUX1
LAUX1
RAUX2
LAUX2
RMIC
LMIC
MONOIN
ROUT
LOUT
MONOOUT

AUDIO INTERFACE

VC
10   0.1

VREF
10   0.1

RMIXOUT0
RMIXOUT1   0.47
LMIXOUT0
LMIXOUT1   0.47

SERIAL EEPROM (256B)

SCK
SDA
WC#

RWA030 INTERFACE

XCLK (MHZ50)	XCLK
YCLK (MHZ25)	YCLK
HSIFI	HSIFI
HSIFO	HSIFO
SADATAI	SADATAI
SADATAO	SADATAO
BCLK	BCLK
LRCLK	LRCLK
SDOUT	SDIN
WRESET#	RESETP

*SA[15:0] for RWA010
SA[11:0] for RWA011

MD152F2 RWA010 IF

Figure 3-1. RWA010 Interface Signals
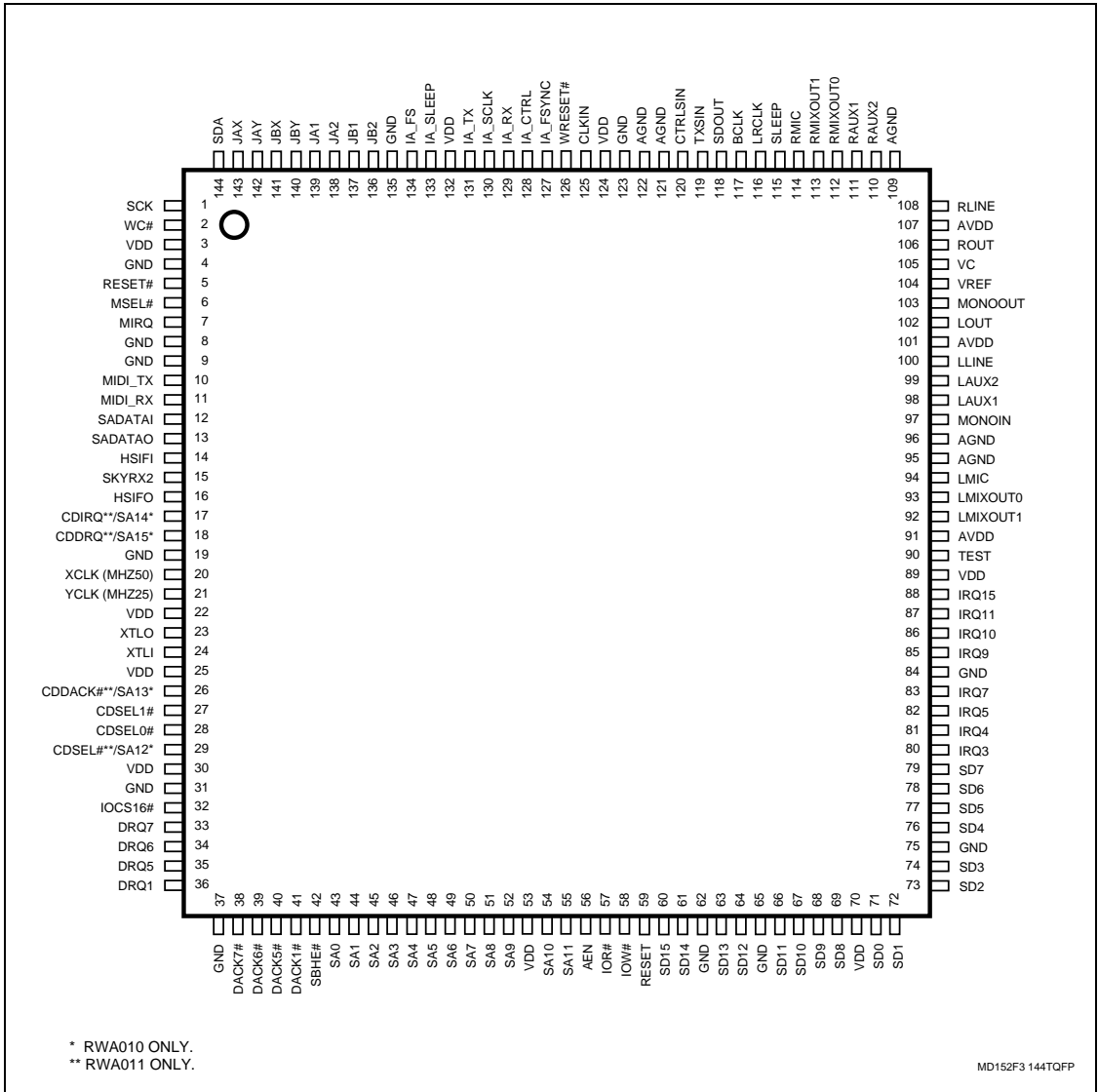
Figure 3-2. RWA010 Pin Signals – 144-Pin PQFP

* RWA010 ONLY.
** RWA011 ONLY.

MD152F3 144TQFP

Table 3-1. RWA010 Hardware Interface Signal Definitions

Label	Pin No.	I/O	Type	Signal/Definition
General				
XTLI XTLO	24 23	I, O	Ixtl, Oxtl	**Crystal Input, Crystal Output.** Connect to a 50.8032 MHz crystal circuit.
VDD	3, 22, 25, 30, 53, 70, 89, 124, 132	I	PWR	**Digital Power.** Connect to +5 VDC.
AVDD	91, 101, 107	I	PWR	**Analog Power.** Connect to +5 VA.
GND	4, 8-9, 19, 31, 37, 62, 65, 75, 84, 123, 135	O	GND	**Digital Ground.** Connect to digital ground.
AGND	95-96, 109, 121, 122	O	GND	**Analog Ground.** Connect to analog ground.
SKYRX2	15	I	Itpd	**NC.**
TEST	90	I	Itpd	**Test.** NC.
Host Bus Interface				
AEN	56	I	It	**Host Bus Address Enable.** Active high input asserted during a DMA cycle. The PnP logic responds to the host address bus and I/O command signal lines (IOR# or IOW#) when AEN is low.
SA[15:12] (RWA010 only), SA[11:0]	18-17, 26, 29, 55-54, 52-43	I	It	**Host Bus Address Lines.** Host address bus lines used for PnP ADDRESS, WRITE_DATA, READ_DATA ports and I/O Port Base decoding. All I/O and PnP registers are decoded with 16 bits (RWA010) or 10 bits (RWA011).
SD[15:0]	60-61, 63-64, 66-69, 79-76, 74-71	I/O	It/Ot12	**Host Bus Data Lines.** Host bus bidirectional data lines used to transfer data between the host and the RWA010.
IOR#	57	I	Itst	**Host Bus Read.** Active low input asserted to strobe read data from the RWA010 onto the host data bus (SD[15:0]). This pin has an internal 100k Ω pull-up resistor.
IOW#	58	I	Itst	**Host Bus Write.** Active low input asserted to strobe write data from the host data bus (SD[15:0]) into the RWA010. This pin has an internal 100k Ω pull-up resistor.
IRQ[15, 11, 10, 9, 7, 5, 4, 3],	88-85, 83-80	O	Otts8	**Interrupt Request.** Active high output asserted to indicate an interrupt request by the RWA010.
DRQ1, DRQ5, DRQ6, DRQ7	36-33	O	Otts8	**DMA Request.** Active high output asserted to request DMA data transfer.
DACK1#, DACK5#, DACK6#, DACK7#	41-38	I	It	**DMA Request Acknowledge.** Active low input asserted to acknowledge the corresponding DMA request.
RESET	59	I	Itst	**Host Reset.** Active high input asserted to reset the RWA010. When asserted, all internal registers are reset to their hardware default states. The pin must be asserted at least 10 ms before being deasserted. While in the reset state, all host bus activity is ignored.
IOCS16#	32	O	Otod12	**I/O 16.** Active low output asserted during an I/O read or write operation. This pin is an open collector output driver.
SBHE#	42	I	It	**System Bus High Enable.** Active low input asserted when the high-order byte of the host bus is to be accessed.

Table 3-1. RWA010 Hardware Interface Signal Definitions

Label	Pin No.	I/O		Signal/Definition
Serial EEPROM Interface
SCK	1	O	Ot2	**Serial EEPROM Clock.** 400 kHz clock timing output to a 24C02 serial EEPROM.
SDA	144	I/O	It/Otod2	**Serial EEPROM Address/Data I/O.** Bidirectional data bit to and from a 24C02 serial EEPROM. Connect this pin to an external pull-up resistor (e.g., 10 kΩ) to VCC.
WC#	2	O	Ot2	**Serial EEPROM Write Control.** Active low output to allow writing into the EEPROM memory.
Modem Controller Interface
MSEL#	6	O	Ot2	**Modem Chip Select.** Active low output to the modem controller asserted whenever a valid address is present on host address bus, i.e., an address which falls within the I/O range written by the host bus to the I/O Space Configuration Register.
MIRQ	7	I	Itpd	**Modem Interrupt Request.** Active high input from the modem's HINT pin.
RESET#	5	O	Ot2	**Modem Reset.** Active low output; inverse of RESET from the host bus. This signal is used to reset the modem controller and the CD-ROM interface.
Game Port and MIDI Port Interface
JA1 JA2	139 138	I	Itpu1k	**Joystick A Switch Inputs 1 and 2.** Binary inputs used to determine the state of Joystick A switches 1 and 2. These ports each have a built-in 10 kΩ pull-up resistor.
JAX JAY	143 142	I	Ia/Ocod12	**Joystick A X-Y Position.** Analog inputs used to determine the position of the Joystick A potentiometer.
JB1 JB2	137 136	I	Itpu1k	**Joystick B Switch Inputs 1 and 2.** Binary inputs used to determine the state of Joystick B switches 1 and 2. These ports each have a built-in 10 kΩ pull-up resistor.
JBX JBY	141 140	I	Ia/Ocod12	**Joystick B X-Y Position.** Analog inputs used to determine the position of the Joystick B potentiometer.
MIDI_RX	11	I	Itpu	**MIDI Receive.** MIDI serial input data from the MPU-401 UART compatible interface. This pin has a built-in 100 kΩ pull-up resistor.
MIDI_TX	10	O	Ot2	**MIDI Transmit.** MIDI serial output data to the MPU-401 UART compatible interface.
Audio Interface
LAUX1 RAUX1	98 111	I	Ia	**Auxiliary Input 1 Left and Right.**
LAUX2 RAUX2	99 110	I	Ia	**Auxiliary Input 2 Left and Right.**
LLINE RLINE	100 108	I	Ia	**Line-Level Input Left and Right.**
LMIC RMIC	94 114	I	Ia	**Microphone Input Left and Right.**
LOUT ROUT	102 106	O	Oa	**Line-Level Output Left and Right.**
MONOIN	97	I	Ia	**Monaural Input.**
MONOOUT	103	O	Oa	**Monaural Output.**
Audio Interconnect and Reference Voltage
VC	105	REF	REF	**Centerpoint Voltage.** Connect to analog ground through 0.1 μF capacitor and 10 μF capacitor in parallel.
VREF	104	REF	REF	**Reference Voltage.** Connect to analog ground through 0.1 μF and 10 μF in parallel.
LMIXOUT0 LMIXOUT1	93 92	DI	DI	**Mixer Out Coupling Left.** Connect LMIXOUT0 to LMIXOUT1 though an external 0.47 μF capacitor.
RMIXOUT0 RMIXOUT1	112 113	DI	DI	**Mixer Out Coupling Right.** Connect RMIXOUT0 to RMIXOUT1 though an external 0.47 μF capacitor.

Table 3-1. RWA010 Hardware Interface Signal Definitions

Label	Pin No.	I/O	Type	Signal/Definition
CD-ROM Interface (RWA011 Only)				
CDSEL#	29	O	Ot2	**CD-ROM Chip Select.**
CDSEL0#	28	O	Ot2	**CD-ROM Chip Select 0.**
CDSEL1#	27	O	Ot2	**CD-ROM Chip Select 1.**
CDIRQ	17	I	Itpd	**CD-ROM Interrupt Request.**
CDDRQ	18	I	Itpd	**CD-ROM DMA Request.**
CDDACK#	26	O	Ot2	**CD-ROM DMA Request Acknowledge.**
RWA010 Interconnect				
SLEEP	115	DI	DI	Connect to IA_SLEEP.
TXSIN	119	DI	DI	Connect to IA_TX.
CLKIN	125	DI	DI	Connect to IA_FS.
CTRLSIN	120	DI	DI	Connect to IA_CTRL.
IA_SLEEP	133	DI	DI	Connect to SLEEP.
IA_TX	131	DI	DI	Connect to TXSIN.
IA_FS	134	DI	DI	Connect to CLKIN.
IA_CTRL	128	DI	DI	Connect to CNTLSIN.
IA_FSYNC	127	DI	DI	Connect to LRCLK.
IA_RX	129	DI	DI	Connect to SDOUT.
IA_SCLK	130	DI	DI	Connect to BCLK.
RWA030 Interface and Associated RWA010 Interconnect				
XCLK (MHZ50)	20	O	Oc1	**50 MHz Clock.** Connect to RWA030 XCLK.
YCLK (MHZ25)	21	O	Oc1	**25 MHz Clock.** Connect to RWA030 YCLK.
SADATAI	12	O	Ot2	**Serial Audio Data In.** Connect to RWA030 SADATAI input.
SADATAO	13	I	Itpd	**Serial Audio Data Out.** Connect to RWA030 SADATAO output.
LRCLK	116	O	Ot1	**Left/Right Clock for Serial Audio Data.** Connect to RWA030 LRCLK and to RWA010 IA_FSYNC.
BCLK	117	O	Ot1	**Bit Clock for Serial Audio Data.** Connect to RWA030 BCLK and to RWA010 IA_SCLK.
HSIFI	14	O	Ot2	**High Speed Serial Interface Input.** Connect to RWA030 HSIFI.
HSIFO	16	I	Itpd	**High Speed Serial Interface Output.** Connect to RWA030 HSIFO.
SDOUT	118	O	Ot1	**Sampled Data Out.** Connect to RWA030 SDIN and to RWA010 IA_RX.
WRESET#	126	O	Ot2	**Reset.** Active low. Connect to RWA030 RESET.

Notes:

I/O: I = Input, O = Output, DI = Device Interconnect.

I/O Type: See Table 3-2.

No connection (NC) means no external connection allowed (pin may be connected to internal circuitry).

Table 3-2. Input/Output Type Descriptions

Type	Description
DI	Device interconnect, electrical characteristics may not be stated.
Ia	Analog input.
It	Digital input, TTL compatible.
Itpd	Digital input, TTL compatible, internal 50KΩ (typical) pull-down resistor to ground. If not externally driven, the input assumes a low state.
Itpu	Digital input, TTL compatible, internal 50KΩ (typical) pull-up resistor to VDD. If not externally driven, the input assumes a high state.
Itpu1k	Digital input, TTL compatible, internal 1KΩ pull-up resistor (typically 50KΩ) to VDD. If not externally driven, the input assumes a high state.
Itst	Digital input, TTL compatible, schmitt trigger.
Oa	Analog output, see signal analog characteristics.
Oc1	Digital output, CMOS compatible, 1 mA.
Ocod12	Digital output, CMOS compatible, open drain, 12 mA, limited slew rate.
Ot1	Digital output, TTL compatible, 1 mA.
Ot2	Digital output, TTL compatible, 2 mA.
Otod2	Digital output, TTL compatible, open drain, 2 mA.
Otod12	Digital output, TTL compatible, open drain, 12 mA.
Otts8	Digital output, TTL compatible, tristate, 8 mA.
NC	No external connection allowed (pin may be connected to internal circuitry).
Notes: 1. See electrical characteristics in Table 3-3 (digital signals), Table 3-4 (analog input signals), and Table 3-5 (analog output signals). 2. TTL compatible inputs will accept a voltage of $\geq$ 2.0 volts as a logic one level and a voltage of $\leq$ 0.8 volts as a logic zero level.	

Table 3-3. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage TTL	V_{IH}	2.0	–	VDD + 0.3	VDC	
Input Low Voltage TTL	V_{IL}	–0.3	–	0.8	VDC	
Input High Current	I_{IH}			40	µA	V_{IN} = 5.25V, V_{CC} = 5.25V,
Input Low Current	I_{IL}			400	µA	V_{CC} = 5.25V
Input Leakage Current TTL	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0.8V to (VDD-1V)
Output High Voltage TTL	V_{OH}	2.4	–	–	VDC	I_{LOAD} = – 100 µA
Output Low Voltage TTL	V_{OL}	–	–	0.4	VDC	I_{LOAD} = See Table 3-2.
Notes: 1. Test Conditions: VCC = 5V ± 5%, TA = 0°C to 70°C, (unless otherwise stated).						

Table 3-4. ADC Analog Performance

Parameter	Symbol
ADC Resolution	16 bits

Instantaneous Dynamic Range
    LINE Input
    MIC Input
	
	85 dB (typ.)
	74 dB (typ.)

Total Harmonic Distortion (THD)
    LINE Input
    MIC Input
	
	-74 dB (typ.)
	-74 dB (typ.)

Channel Isolation
    LINE-to-LINE
    LINE-to-MIC, LINE-to-AUX 1, and LINE-to-AUX 2
	
	80 dB (min.)
	60 dB (min.)

Channel Gain Mismatch
    LINE input
    MIC input
	
	±0.5 dB (max.)
	±0.5 dB (max.)

Input Gain	0.0 dB to 22.5 dB (typ.) [in 1.5 dB steps]
ADC Path Offset Voltage	±70 LSB (typ.)
Gain Error	7% (max.)
Gain Drift	100 ppm/°C

Full Scale Input
    LINE, AUX 1, AUX 2, MONOIN
    MIC input (±0 dB)
    MIC input (±20 dB)
	
	2.9 Vp-p (max.)
	2.9 Vp-p (max.)
	290 mVp-p (max.)

Input Resistance	30 kΩ (min.), 200 kΩ (max)
Input Capacitance	5 pF (typ.)
Test Conditions: VCC = ±5 V, TA = 25°C; Input: 1 kHz sine wave; Conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; 16-bit linear coding; dynamic range measured for -60 dBV input; THD measured for 1 Vrms input; nominal gain = 0 dB.	

Table 3-5. DAC Analog Performance

Parameter	Symbol
DAC Resolution	16 bits
DAC Differential Non-linearity	± 0.5 LSB (max.)
Total Dynamic Range	85 dB (typ.)
Total Harmonic Distortion (THD) Bypassing Mixer	 -74 dB (typ.)
Channel Isolation LOUT to ROUT	 >-90 dB

Reference Voltage
    Voltage (reference to VC)
    Load Current
	
	1.6 Vdc (Typ.) +VC = 4.0V (VC = 2.5V)
	20 µA (max.)

DAC Offset Voltage	30 mV (typ.), ±50 mV LSB (max.)
Full Scale Output Voltage	2.9 Vp-p (max.)
Gain Drift	3000 ppm/°C
Deviation from Linear Phase	5° (max.)

Output Load Resistance
    LOUT and ROUT
    MONOOUT
	
	10k Ω (min.)
	10k Ω (min.)

Mute Attenuation	80 dB (min.) [for 0 dB signal level]
Pass-band Ripple	±0.1 dB (max.)
Out-of-Band Energy (0.6*FS to 3 MHz)	-45 dB (max.)
Audible Out-of-Band Level (0.6*FS to 22 kHz)	-60 dB (max.)
Test Conditions: VCC = ±5 V, TA = 25°C; Output: 1 kHz sine wave; Conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; 16-bit linear coding; dynamic range measured for -60 dBV input; THD measured for 1 Vrms output; nominal gain = 0 dB.	

3.2 Hardware Interface Circuits

This section describes typical WaveArtist interface circuits and connections. Consult the following AccelerATor Kits or reference designs for full schematics of typical applications:

AK28-D680: ACFSP + RWA010/RWA011 Audio/Telephony Internal PC Card

3.2.1 ISA Host Bus Plug and Play (PnP) Interface

The PnP interface supports six logical devices with programmable I/O base address assignments. The logical devices are typically assigned to WaveArtist command/status registers, Sound Blaster Pro, MPU-401, modem, CD-ROM (RWA011 only), and game port. The address assignment, IRQ, DRQ, and DACK signal routing are established by a software driver writing to configuration registers after successful PnP isolation.

Control lines supported are: I/O Read (IOR#), I/O Write (IOW#), Address Enable (AEN), Reset (RESET), and System Bus High (SBHE#) inputs, and I/O 16 (IOCS16#) output.

Interrupt servicing is supported by eight Interrupt Request outputs (IRQ[15, 11, 10, 9, 7, 5, 4, 3]).

Direct memory access (DMA) is supported by four DMA Request outputs (DMA[7, 6, 5, 1]) and four DMA Acknowledge inputs (DACK#[7,6,5,1]).

The RWA010 address, data, and control signals connect directly to the ISA host bus without the need for external glue logic.

3.2.2 PnP Serial EEPROM Interface

A 3-line serial interface to a XICOR X24C02 or compatible serial EEPROM is supported. The interface signals are the Data Clock (SCK) and Write Control (WC#) outputs and a bidirectional Serial Data (SDA) line. Since the SDA interface is open collector, an external 10 KΩ pullup resistor to VCC is required.

A DOS utility is available for programming the EEPROM from the host bus.

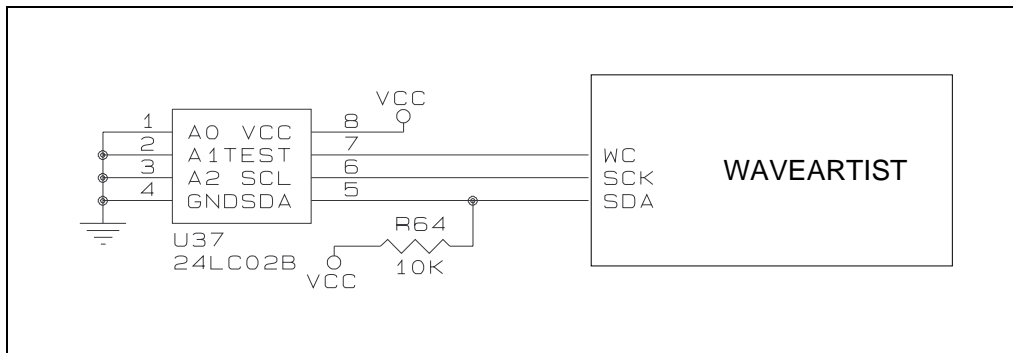A typical EEPROM interface connection is shown in Figure 3-3.

Figure 3-3. Typical EEPROM Interface Connection

3.2.3 Audio Interface

Stereophonic signals supported are: Microphone (RMIC, LMIC), Line In (RLINE, LLINE), CD Audio In (RAUX1, LAUX1), and Auxiliary 2 In (RAUX2, LAUX2) inputs and Audio Out (ROUT, LOUT) outputs. Monophonic signals supported are: Mono In (MONOIN) input and Mono Out (MONOOUT) output.

Mic In

Two microphone input signals (LMIC and RMIC) are supported. A typical microphone interface is shown in Figure 3-4.

In Figure 3-4, the signal from the microphone receptacle is AC coupled by capacitor C88 to the LMIC and RMIC pins to provide an input to both channels. The signal at LMIC and RMIC is optionally routed to the modem voice mic input (MIC_V) through isolation capacitor C136. This configuration supports both the electret microphone and the Plantronics headset.

No external amplifier is needed for boosting the microphone level since +20 dB is provided by the codec. The +20 dB can be enabled by software control.

A DC bias to an electret microphone is provided by the R123, R124, C143, and C144 circuit. The low side of R124 provides the filtered bias for the microphone and C143 and C144 provide decoupling. The bias current should be less than 0.65 mA for all Plantronics headsets.

High frequency noise is filtered at the microphone receptacle by capacitor C5. EMI noise suppression is provided by ferrite inductor L1.

Figure 3-4. Typical Microphone In Interface Circuit

Line In

Two line-level input signals (LLINE and RLINE) are supported. A typical Line In interface circuit is shown in Figure 3-5.

In Figure 3-5, the left channel input is voltage divided by resistors R89 and R114 to reduce the input voltage to the 1.0 V_{RMS} (2.0 V_{P-P}) maximum input level and then AC coupled by capacitor C82 to the LLINE input pin. Similarly, the right channel input is voltage divided by resistors R91 and R115 then AC coupled by C83 to the RLINE input pin.

High frequency noise is filtered at the Line In receptacle by capacitors C117 and C118. EMI noise suppression is provided by ferrite inductors L20 and L21.
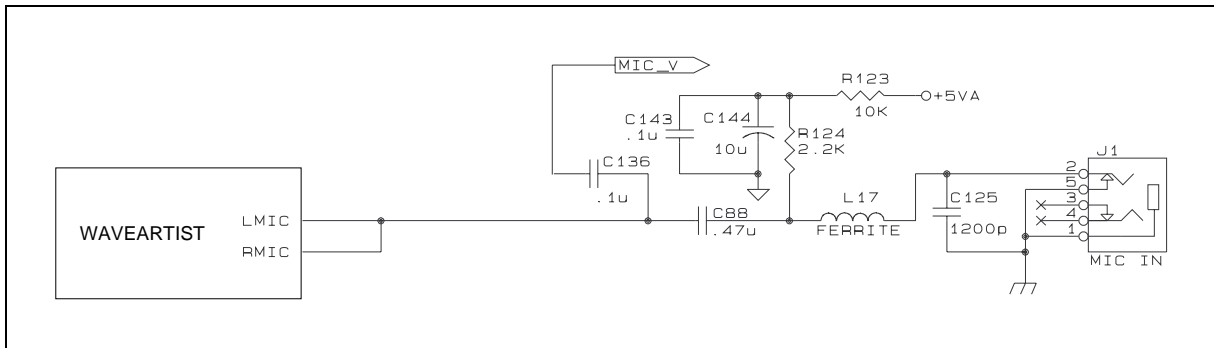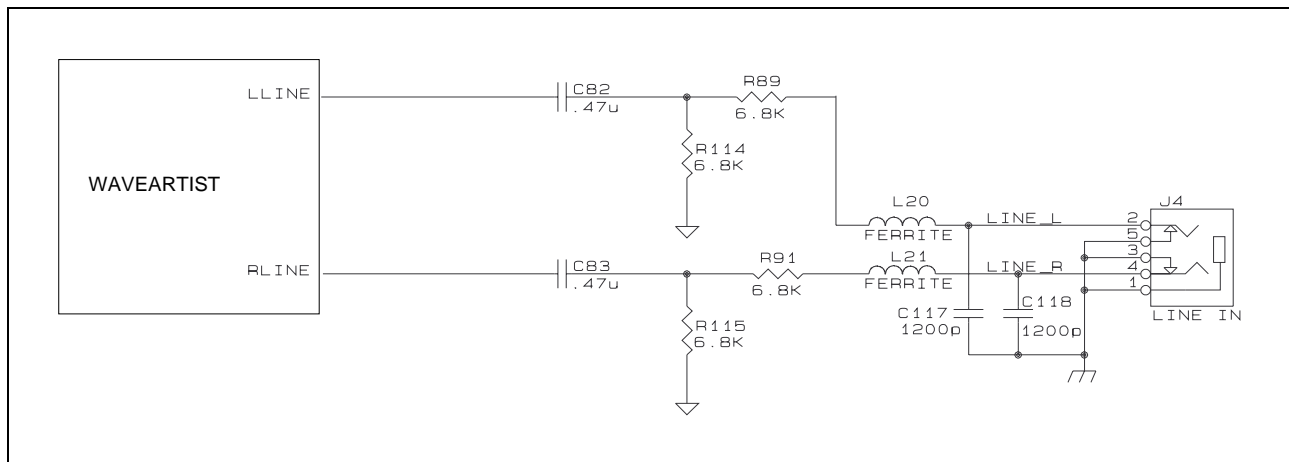

Figure 3-5. Typical Line In Interface Circuit

Aux Input 1

Two auxiliary input 1 signals (LAUX1 and RAUX1) are supported.

A typical Aux Input 1 interface circuit to a CD-ROM is shown in Figure 3-6. In Figure 3-6, the left channel input is voltage divided by resistors R87 and R88 to reduce the input voltage to the 1.0 V_{RMS} maximum input level and then AC coupled by capacitor C85 to the LAUX1 input pin. Similarly, the right channel input is voltage divided by R85 and R86 then AC coupled by C84 to the RAUX1 input pin.
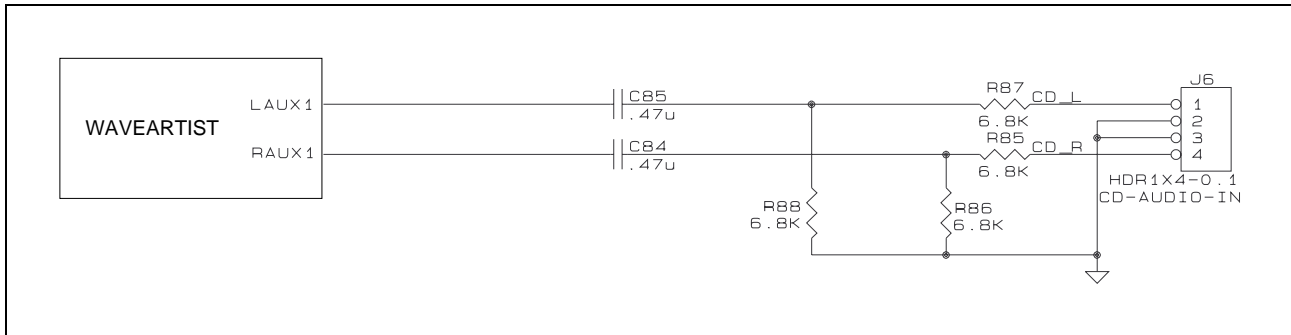
Figure 3-6. Typical Aux Input 1 Interface Circuit

Aux Input 2

Two auxiliary input 2 signals (LAUX2 and RAUX2) are supported. A typical Aux Input 2 interface circuit a modem/telephone line/telephone handset interface is shown in Figure 3-7.

In Figure 3-7, the left channel input from the modem TXA output is AC coupled by capacitor C1 to the LAUX2 input pin. Similarly, the right channel input from the modem voice speaker output (SPK_V) is AC coupled by C2 to the RAUX2 input pin.
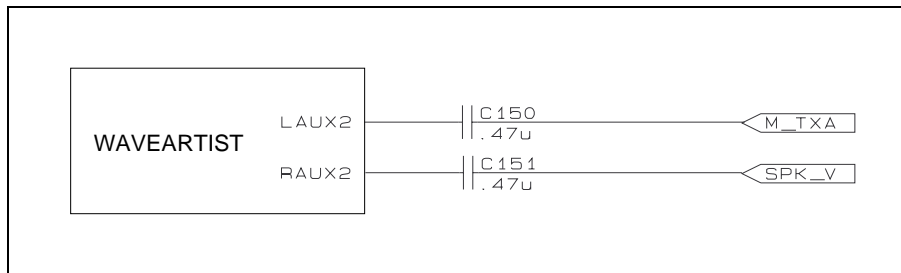
Figure 3-7. Typical Aux Input 2 Interface Circuit

Mono In

A monaural input (MONOIN) is supported. A typical Mono In interface circuit is shown in Figure 3-8.

For a modem voice application, the Mono In input is typically AC coupled through C86 to the modem voice speaker output.

For a PC speaker application, the Mono In input is typically AC coupled to the PC speaker output from a PC motherboard. The PC speaker output signal from the PC motherboard is disconnected from the speaker and connected through a voltage divider to the MONOIN pin. (In this application, MONOOUT is then routed to the speaker connector, see MONOUT description).

a. Modem Voice Speaker In Interface

b. PC Speaker In Interface
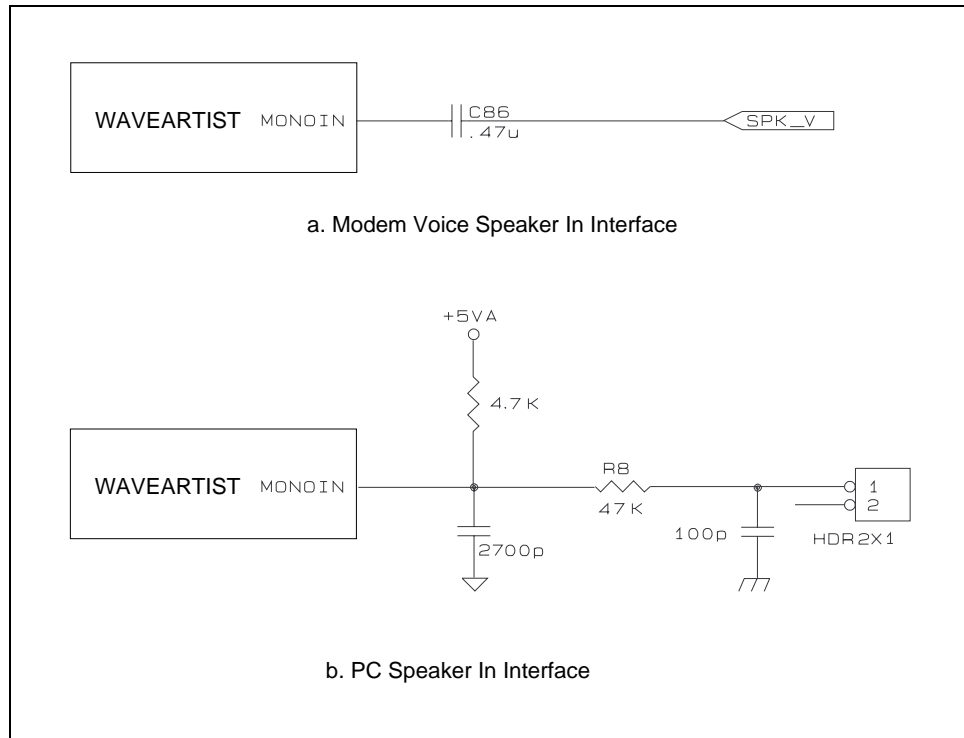
Figure 3-8. Typical Mono In Interface Circuit

Line Out

Two line-level output signals (LOUT and ROUT) are supported. A typical Line Out interface circuit is shown in Figure 3-9.

In Figure 3-9., the LOUT output is AC coupled through capacitor C1 to the left channel of the line out receptacle and to the left channel the headset receptacle through attenuator resistor R1. Likewise, the ROUT output is AC coupled through C2 to the right channel of the line out receptacle and headset receptacle through attenuator resistor R2. The signals are routed through ferrite inductors L1, L2, L3, and l4 for EMI suppression and filtered at the output receptacle by capacitors C3, C4, C5, C6 to chassis ground.
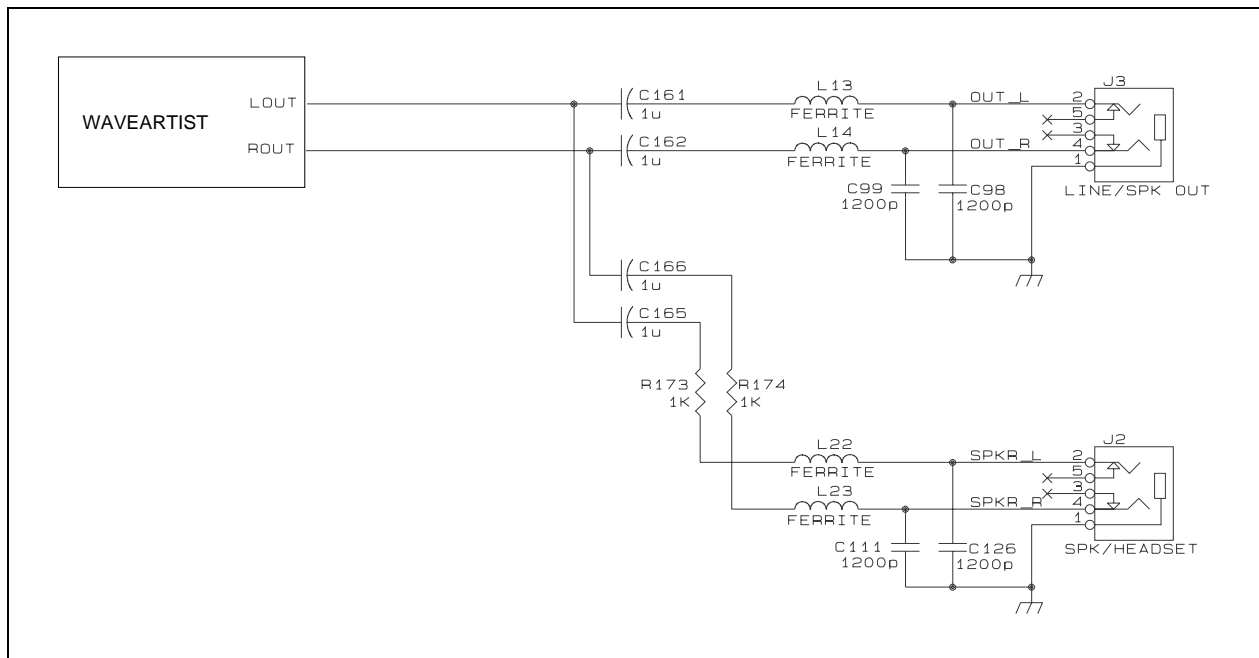
Figure 3-9. Typical Line Out Interface Circuit

Mono Out

A monaural output (MONOOUT) is supported. The MONOOUT signal is a mix of the left and right line out channels and can be independently muted. Typical Mono out interface circuits supporting connection to a PC speaker input or to a modem music input are shown in Figure 3-10.

For the modem music on hold application, the MONOOUT is AC coupled through C89 to the music on hold circuit.

For the PC speaker connection, the MONOOUT signal is AC coupled through 1.0 uF to an amplifier circuit which drives the speaker through a 4-pin header on the motherboard for connection to the speaker lines. (In this application, MONOIN is connected to the PC speaker output signal from the PC motherboard, see MONOIN description).
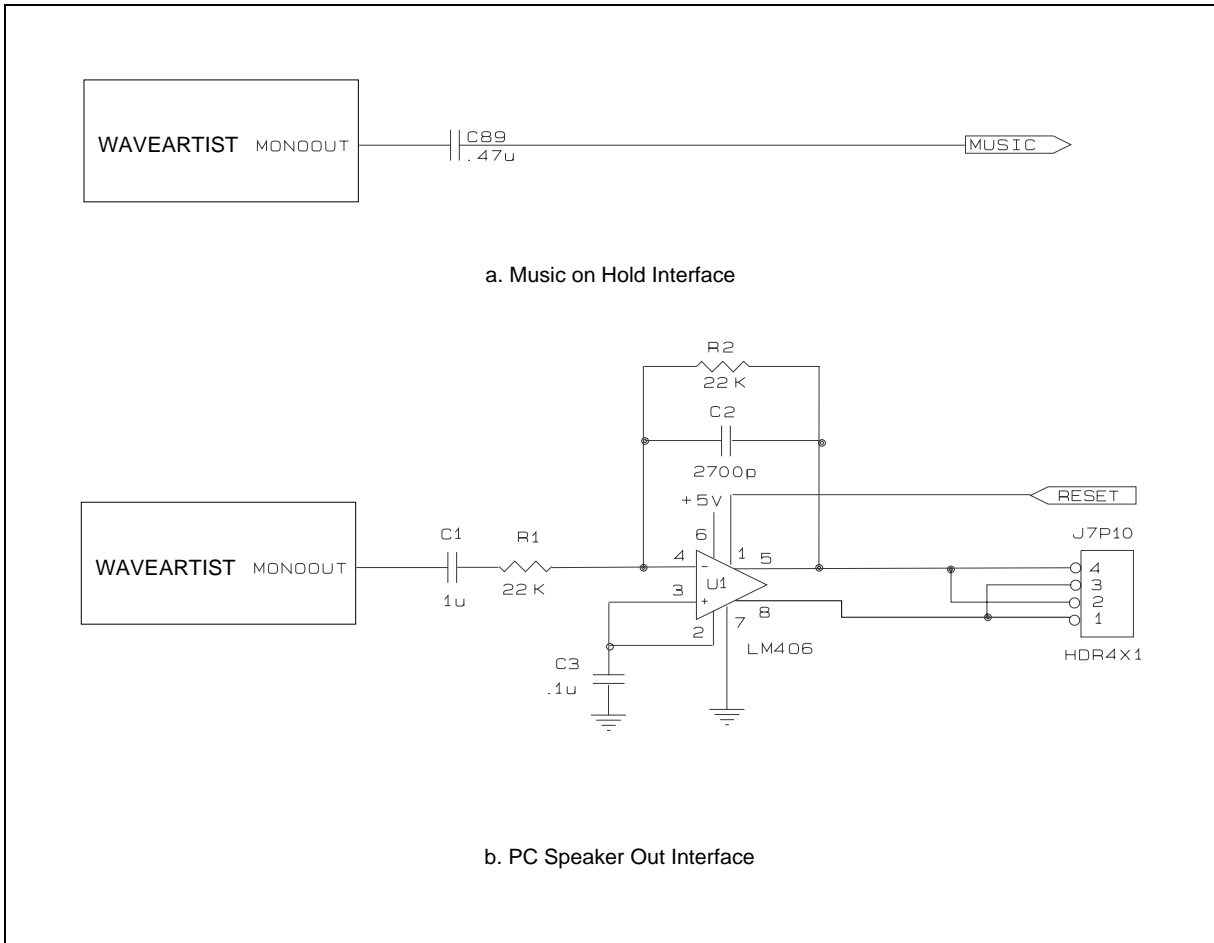
Figure 3-10. Typical Mono Out Interface Circuit

3.2.4 Enhanced IDE CD-ROM Interface

The supported signals are CD-ROM Select output (CDSEL#), two programmable address chip select outputs (CDSEL0# and CDSEL1#), CD-ROM Interrupt Request output (CDIRQ), CD-ROM DMA Request output (CDDRQ), and CD-ROM DMA Request Acknowledge input (CDDACK#). The address base and the IRQ and DMA signal assignments are established via the PnP setup.

A typical CD-ROM interface circuit to a 40-pin CD-ROM header is shown in Figure 3-11.

The 16 CD-ROM data lines (CD15:0]) are routed from the header to the host bus data bus (SD[15:0]) through transceivers U2 (lower 8 bits [7:0]) and U3 (upper 8 bits [15:8]). The lower data byte from the CD-ROM is enabled onto the host bus through transceiver U2 when CDSEL# is low and DIOR# is low (buffered host bus read, IOR#, through buffer U1). The upper data byte from the CD-ROM is enabled onto the host bus through transceiver U3 when ENHI# is low and DIOR# is low.

CDSEL0#, CDSEL1#, CDIRQ, CDDACK# , RESET#, and CDDRQ are routed directly to the header. Pull down resistor R1 is connected to CDDRQ.
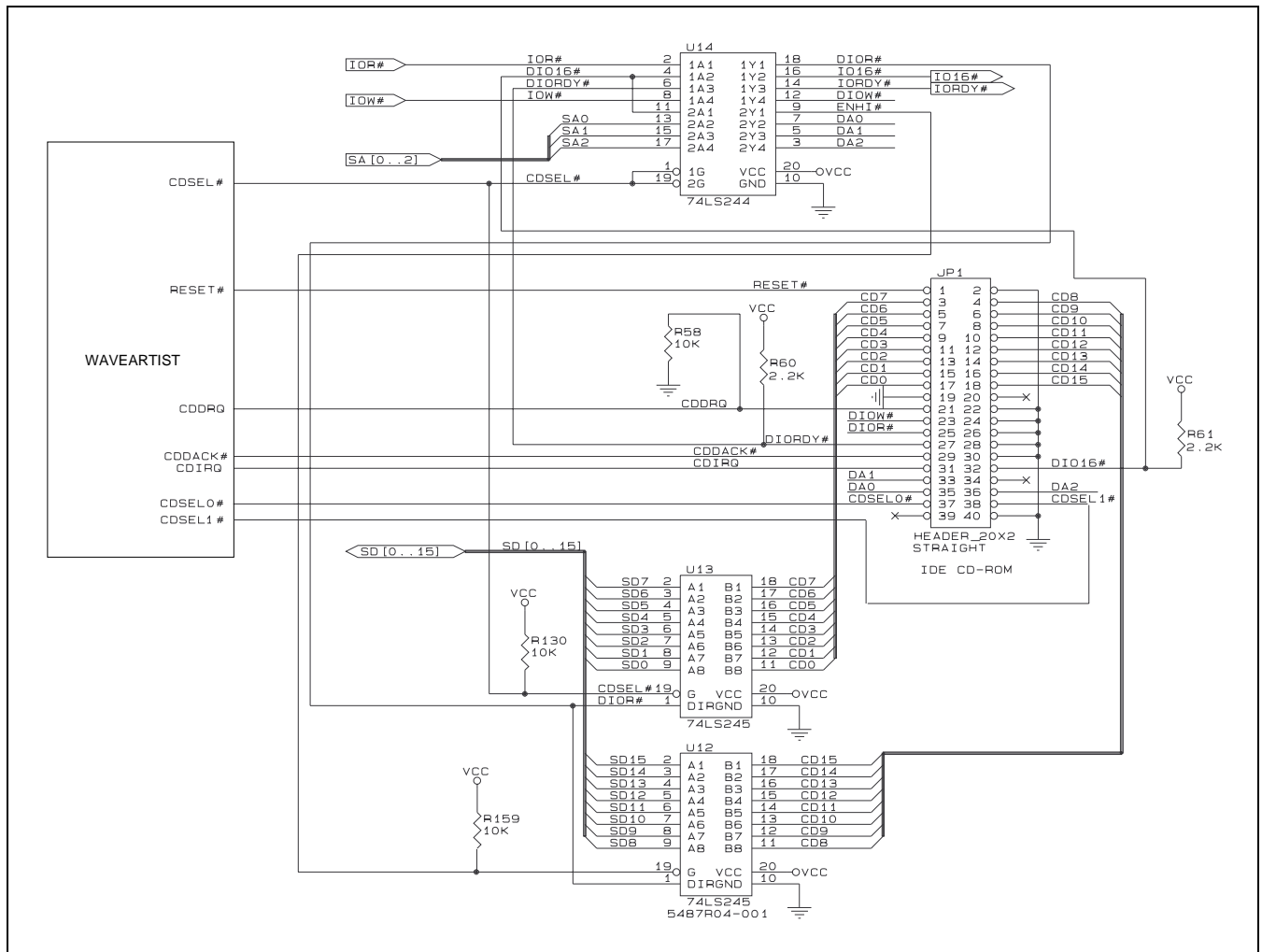
Figure 3-11. Typical CD-ROM Interface Circuit (RWA010)

3.2.5 Joystick/MIDI Interface

Eight joystick and two MIDI signals are supported. These signals are typically routed to a standard 15-pin DB-15 PC game port connector. Only a few external passive components are required to complete the game port interface circuit.

Joystick Interface

The four timer input pins (JAX, JAY, JBX, and JBY) can support two joysticks or four paddles. The four button input pins (JA1, JA2, JB1, and JB2) can support two buttons per joystick. No external timer device is required. A typical joystick/MIDI interface is shown in Figure 3-12.

In Figure 3-12, for the JAX timer input signal, R1 and C1 provide the timer debounce period time constant. C5 and L1 provide high frequency noise suppression, if needed. The JAY, JBX, and JBY signal interface circuits operate identically. When the host PC writes to the game port, the timer pins discharge the external capacitors and set an internal flip-flop output to 1. When the capacitor charges up to the internal threshold voltage (0.63 VCC or one RC time constant), the internal flip-flop is reset to 0. The capacitor charging time constant determined by the joystick potentiometer value and the external R1 C1 circuit. The timer output pin can discharge the 0.1µF capacitor from the falling edge of the internal decoded game write signal to within 400 ns. The host PC will periodically read the game port address for push button status and calculate the X and Y coordinate based on the duration of the timer flip-flop output bit being high.

The JA1 switch input can be routed directly from the DB-15 connector, i.e., no external pullup resistors are required. Capacitor C5 provides switch overshoot protection. The JB1, JA2, and JB2 signal interface circuits operate identically.

Figure 3-12. Typical Joystick/MIDI Interface Circuit

MIDI Interface

The MIDI serial interface can receive and transmit serial data at TTL logic levels. External hardware is required to connect the two signals, MIDI Receive (MIDI_RX) input and MIDI Transmit (MIDI_TX) output, to interface with other MIDI compatible components. The serial data character format consists of one start bit (logical 0), eight data bits (LSB shifted first), and one stop bit (logical 1). The data rate complies with the standard MIDI specification.

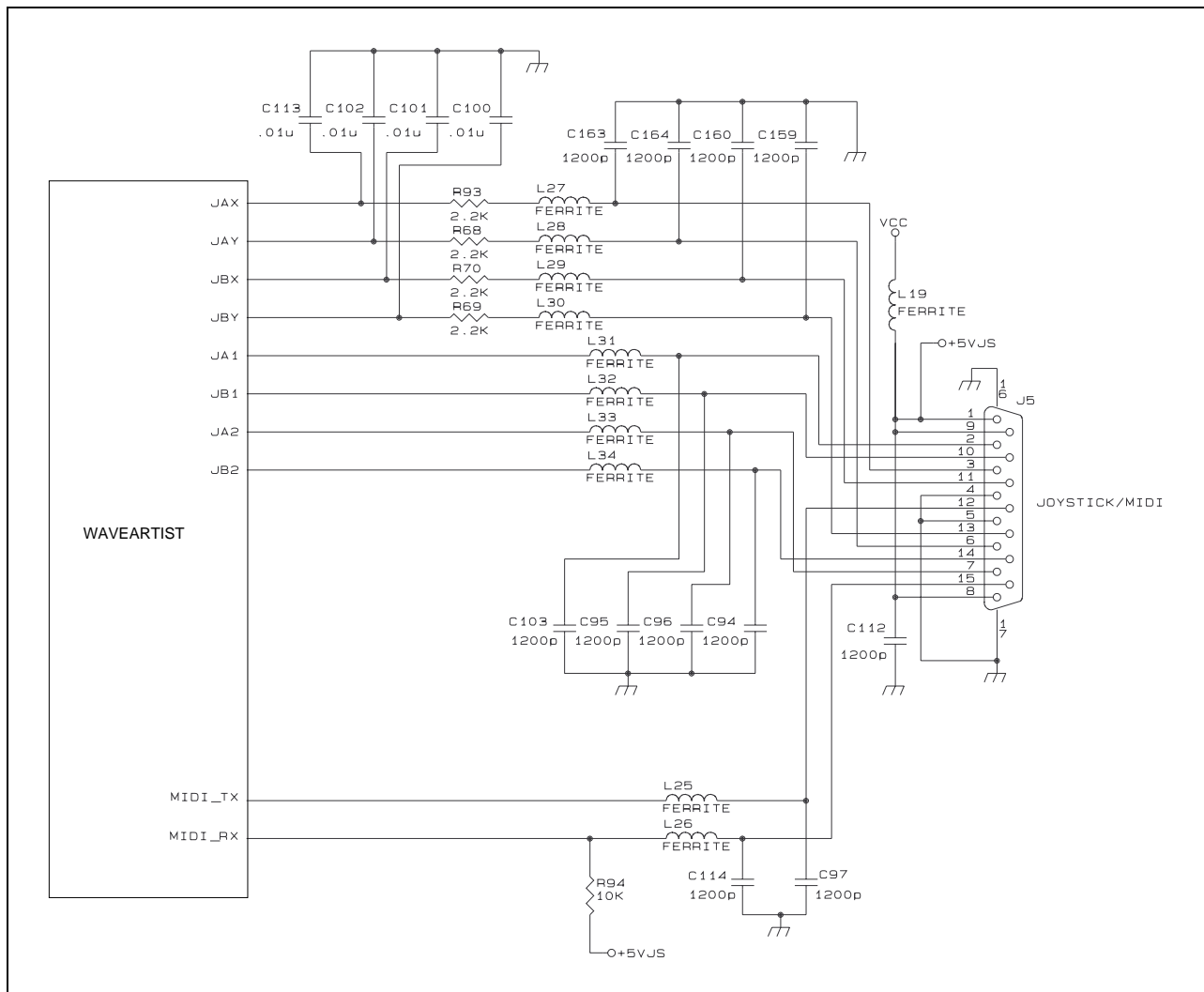In Figure 3-12, MIDI_TX and MIDI_RX signals are routed directly to the DB-15 game connector. A ferrite inductor in each line may be needed for EMI suppression. Each line must be connected to chassis ground through a 1200 pF capacitor.

3.2.6 Modem Interface

Only three signals are needed to connect the WaveArtist to a Rockwell modem: Modem Reset (RESET#) and Modem Chip Select (MSEL#) outputs and Modem Interrupt Request (MIRQ) input. A typical modem connection is shown in Figure 3-13. The RESET# output connects to the Modem ~RESET input, the MSEL# output connects to the modem ~HCS input and to the modem data bus transceiver (U1) G input, and the MIRQ input connects to the modem HINT output.

The MSEL# output is pulled up by R1 to deselect the modem and to disconnect (provide high impedance) the modem data lines from the host bus through the transceiver (U1) when the WaveArtist is not active.

An external pulldown resistor in needed on the MIRQ input.

Note that the modem data lines can normally be connected directly to the data bus transceiver (U1), however, a series resistor may be required in each modem data line in some computers to reduce signal reflections/switching transients on the data bus lines.

The modem host address inputs (HA2:0], host read (~HRD), and host write (~HWT) connect directly to the host bus connector. The address lines are connected to GND through 15 pF capacitors for noise suppression.
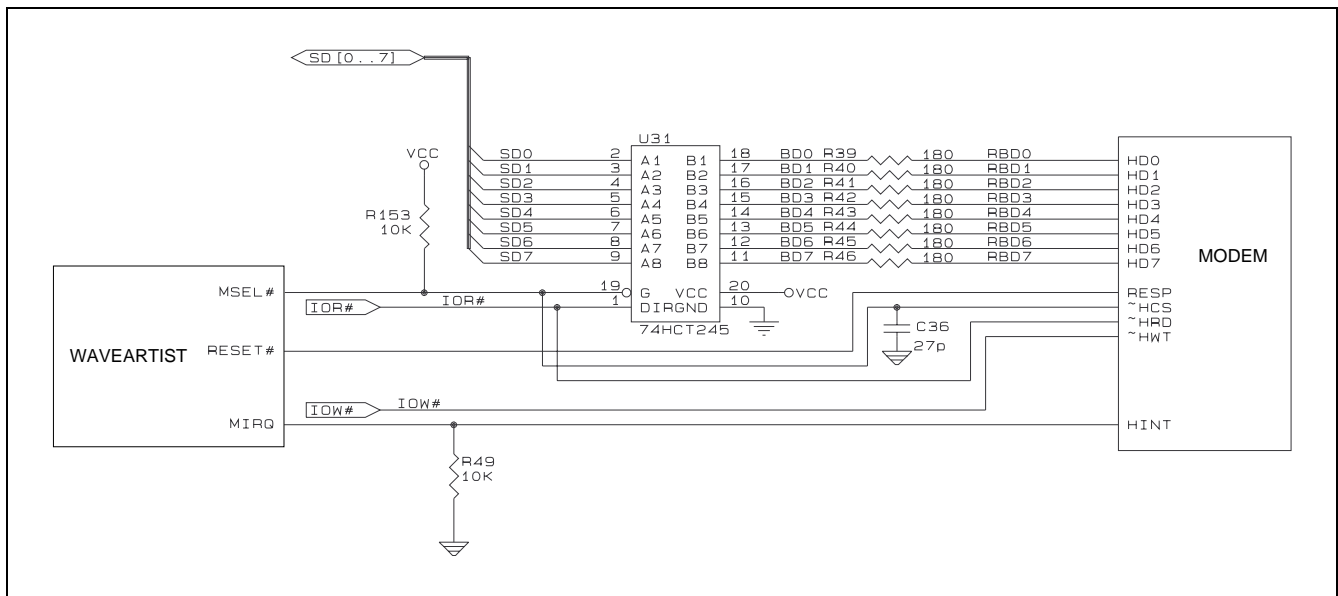
Figure 3-13. Typical Modem Interface Circuit

3.2.7 RWA030 Music Processor Interface

The RWA010 controls the optional RWA030 Music Processor using the Clock (XCLK), Left/Right Clock (LRCLK), Bit Clock (BCLK), and Reset (WRESET#) outputs. Digital audio data is transferred to and from the RWA030 over the Serial Audio Data Out (SADATAO) and Serial Audio Data In (SADATAI) lines. Additional control/status/MIDI information is transferred to and from the RWA030 over the High Speed Interface Out (HSIFO) and the High Speed Interface In (HSIFI) serial lines. Digital samples of the analog audio input signals are also sent to the RWA030 using the Sampled Data Output (SDOUT) line.

3.2.8 Crystal Interface Circuit

See Figure 3-14.
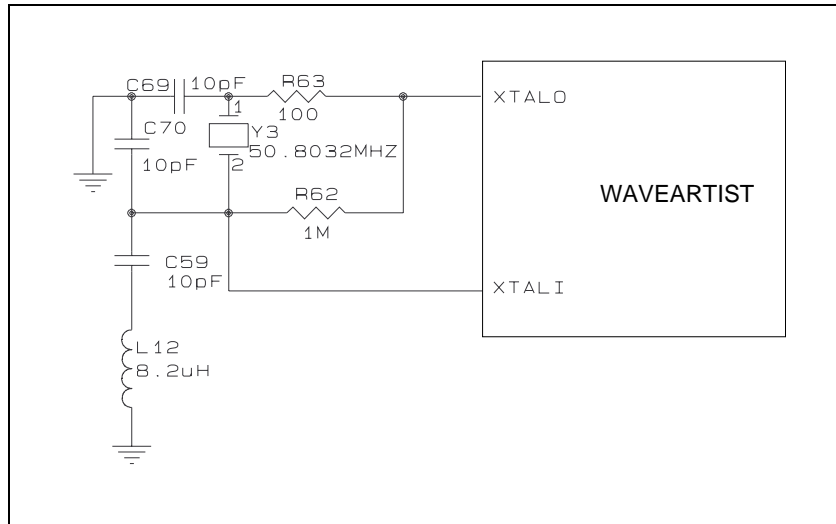
Figure 3-14. Typical Crystal Interface Circuit

4. Interface Timing and Waveforms

4.1 ISA Bus Timing

The ISA system bus interface timing is shown in Figure 4-1 (host write) and Figure 4-2 (host read).

The chip select signal throughput timing is shown in Figure 4-3.

The IRQ signal throughput timing is shown in Figure 4-4.

The DRQ signal throughput timing is shown in Figure 4-5.

The DACK signal throughput timing is shown in Figure 4-6.

Timing Requirements

IOW# pulse width	tww	150 ns min
SAn setup	tsas	45 ns min
SAn hold	tsah	10 ns min
AEN setup	taens	45 ns min
AEN hold	taenh	10 ns min
SDn setup	tws	30 ns min
SDn hold	twh	10 ns min

1104F4-1 HWT
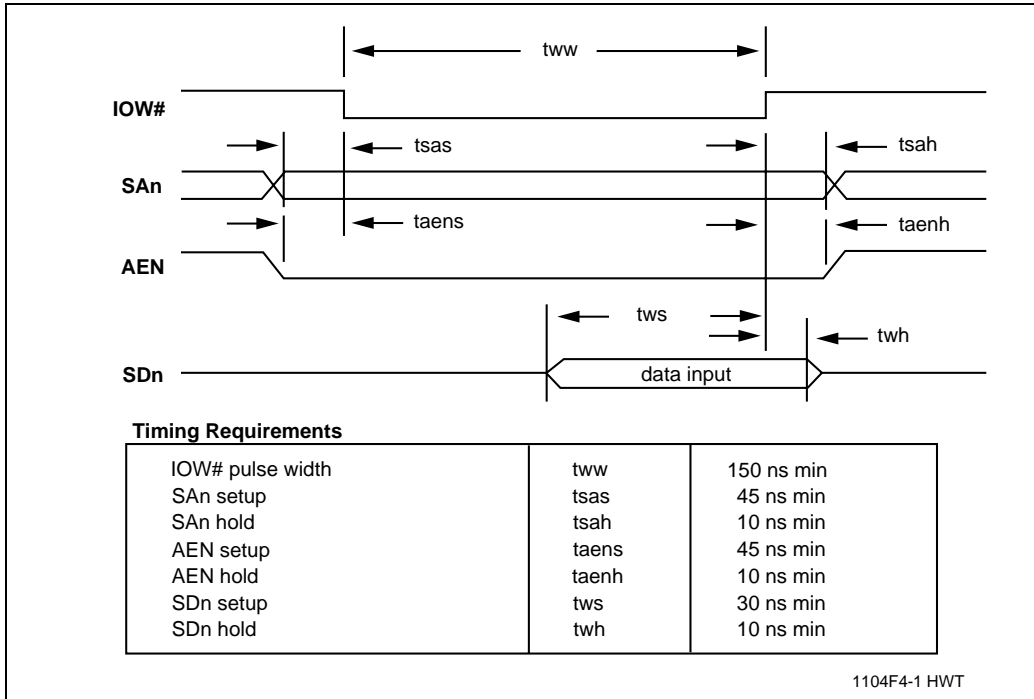
Figure 4-1. Waveforms and Timing – ISA System Write

Timing Requirements

IOR# pulse width	trw	150 ns min
SAn setup	tsas	45 ns min
SAn hold	tsah	10 ns min
AEN setup	taens	45 ns min
AEN hold	taenh	10 ns min
SDn delay	tsrd	50 ns max @150 pF loading
SDn hold	tsrh	0 ns min

1104F4-2-HRD
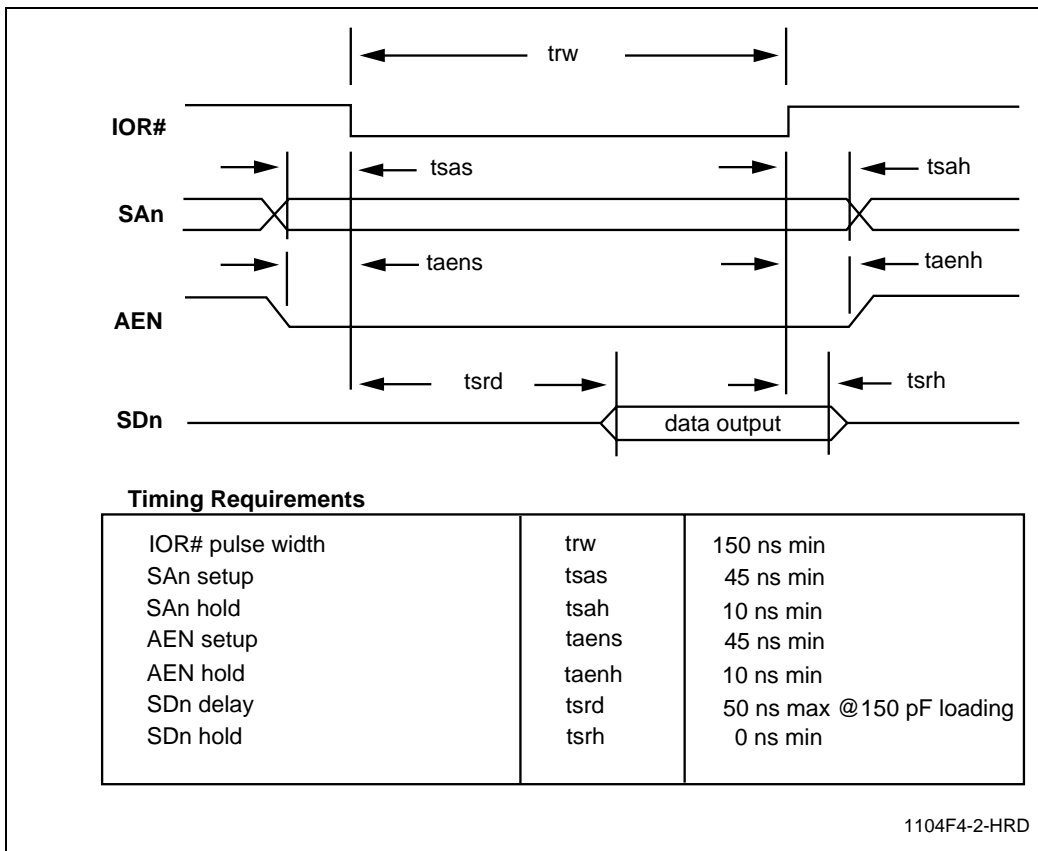
Figure 4-2. Waveforms and Timing – ISA System Bus Read

SAn ——⟨ valid I/O address ⟩——

AEN ————

tcsd   tcsd

MSEL#
CDSEL#
CDSEL0#
CDSEL1#

Timing Requirements

MSEL# delay CDSEL# delay CDSEL0# delay CDSEL1# delay	tcsd	20 ns max @ 50 pF loading

1104F4-3-HCS
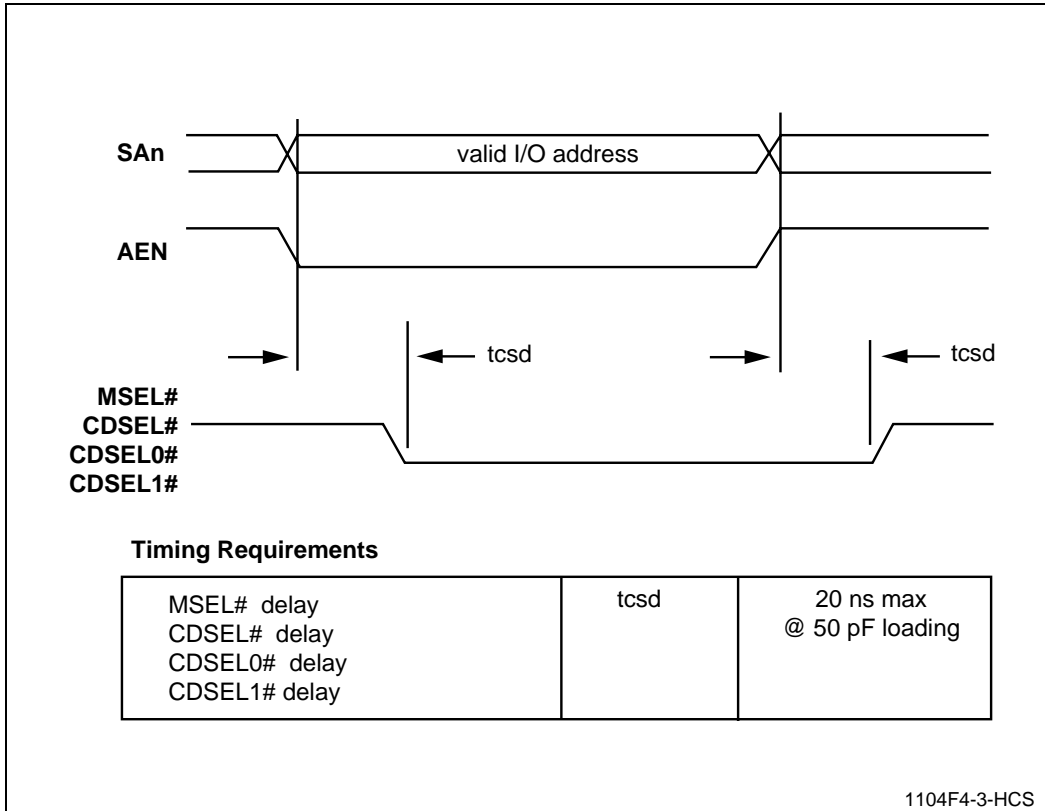
Figure 4-3. Waveforms and Timing – ~Chip Select Throughput Delay

MIRQ
CDIRQ ————

tirqd   tirqd

IRQn ————

Timing Requirements

IRQn delay	tirqd	25 ns max @150 pF loading

1104F4-4 IRQ
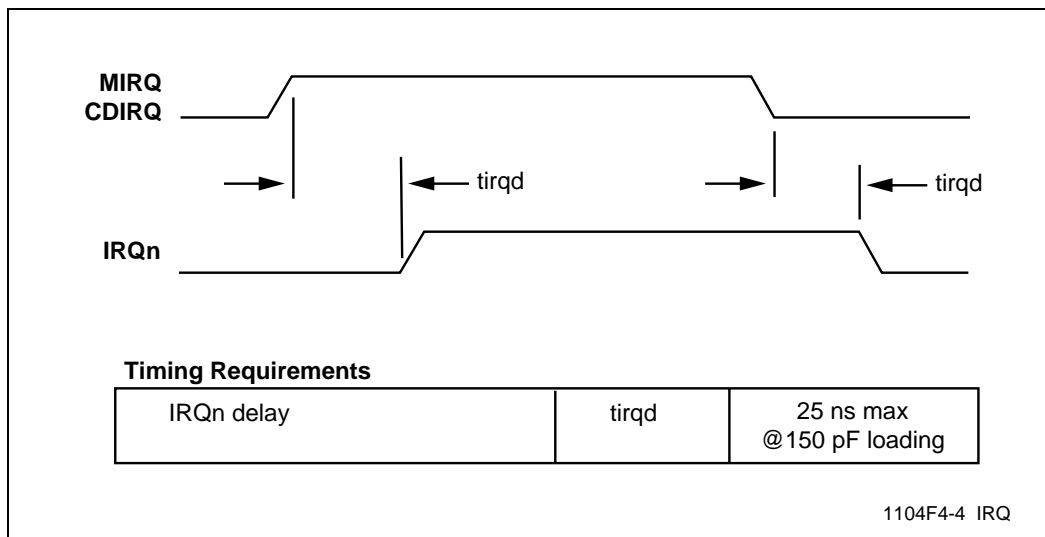
Figure 4-4. Waveforms and Timing – IRQ Throughput Delay
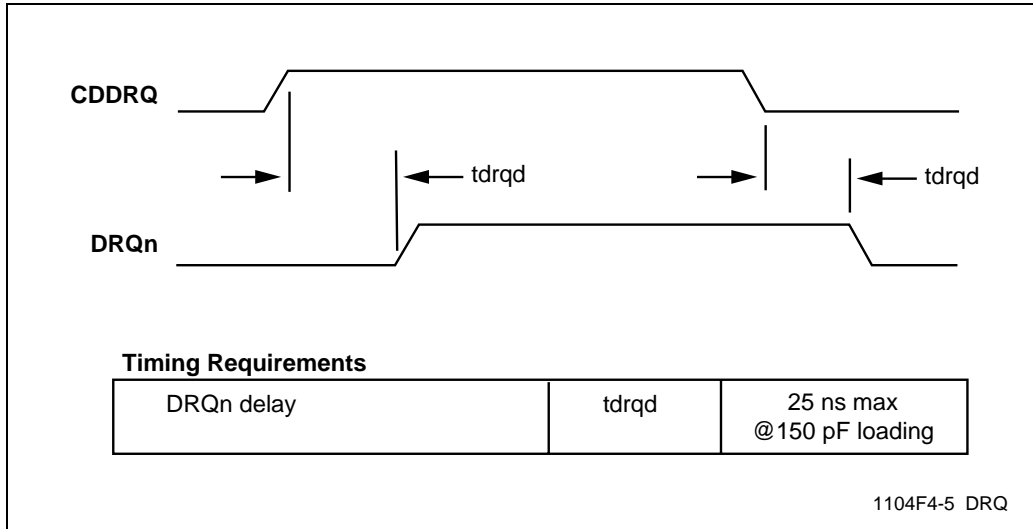
Figure 4-5. Waveforms and Timing – DRQ Throughput Delay

Timing Requirements		
DRQn delay	tdrqd	25 ns max @150 pF loading
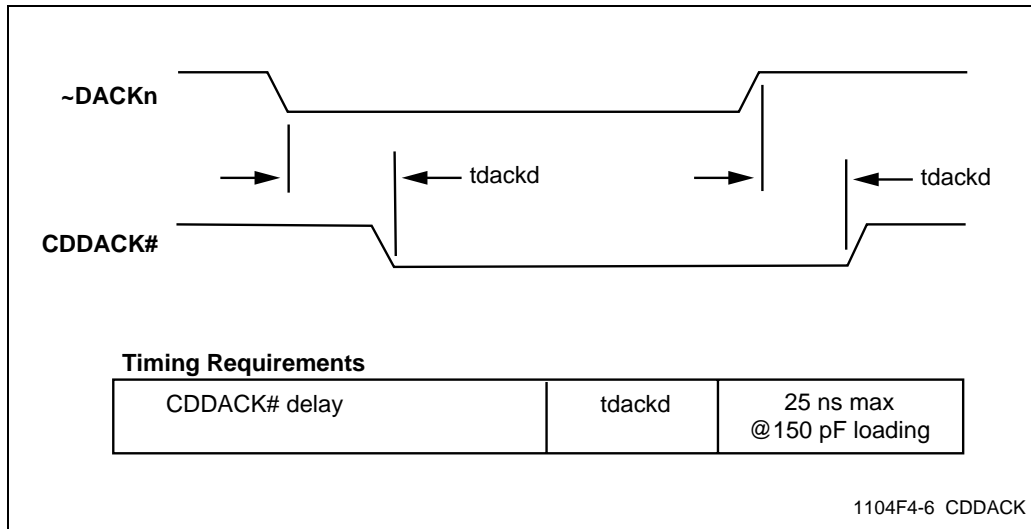
Figure 4-6. Waveforms and Timing – DACK Throughput Delay

Timing Requirements		
CDDACK# delay	tdackd	25 ns max @150 pF loading

4.2 Serial EEPROM Interface Timing

The serial EEPROM interface timing is shown in Figure 4-7 and Table 4-1.

The Serial EEPROM bit format is shown in Figure 4-8.
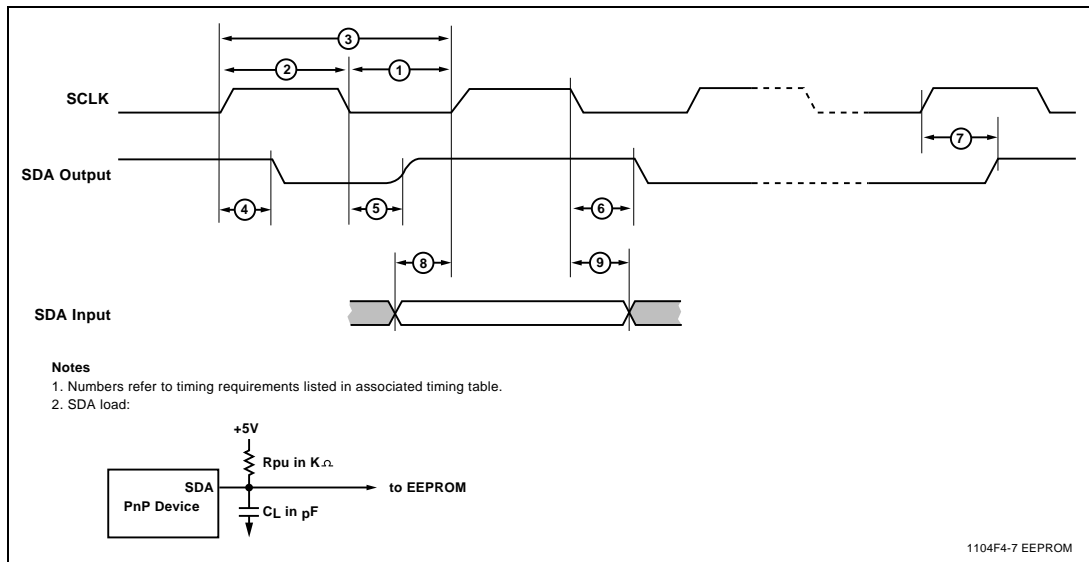
Figure 4-7. Waveforms and Timing – Serial EEPROM Interface

Table 4-1. Timing – Serial EEPROM Interface

Item	Definition	Min.	Max.	Units	Notes
1	SCLK low time	1260	-	ns	Max. load = 100 pF
2	SCLK high time	1260	-	ns	Max. load = 100 pF
3	SCLK clock period	2520		ns	Max. load = 100 pF
4	Start hold after SCLK	630	650	ns	
5	Data output delay (rising)	630	$630 + R_{PU} C_L$	ns	See Figure 4-7, Note 2
6	Data output delay (falling)	630	650	ns	
7	Stop hold after SCLK	630	$630 + R_{PU} C_L$	ns	See Figure 4-7, Note 2
8	Data setup to SCLK	50	-	ns	
9	Data hold after SCLK	0	-	ns	
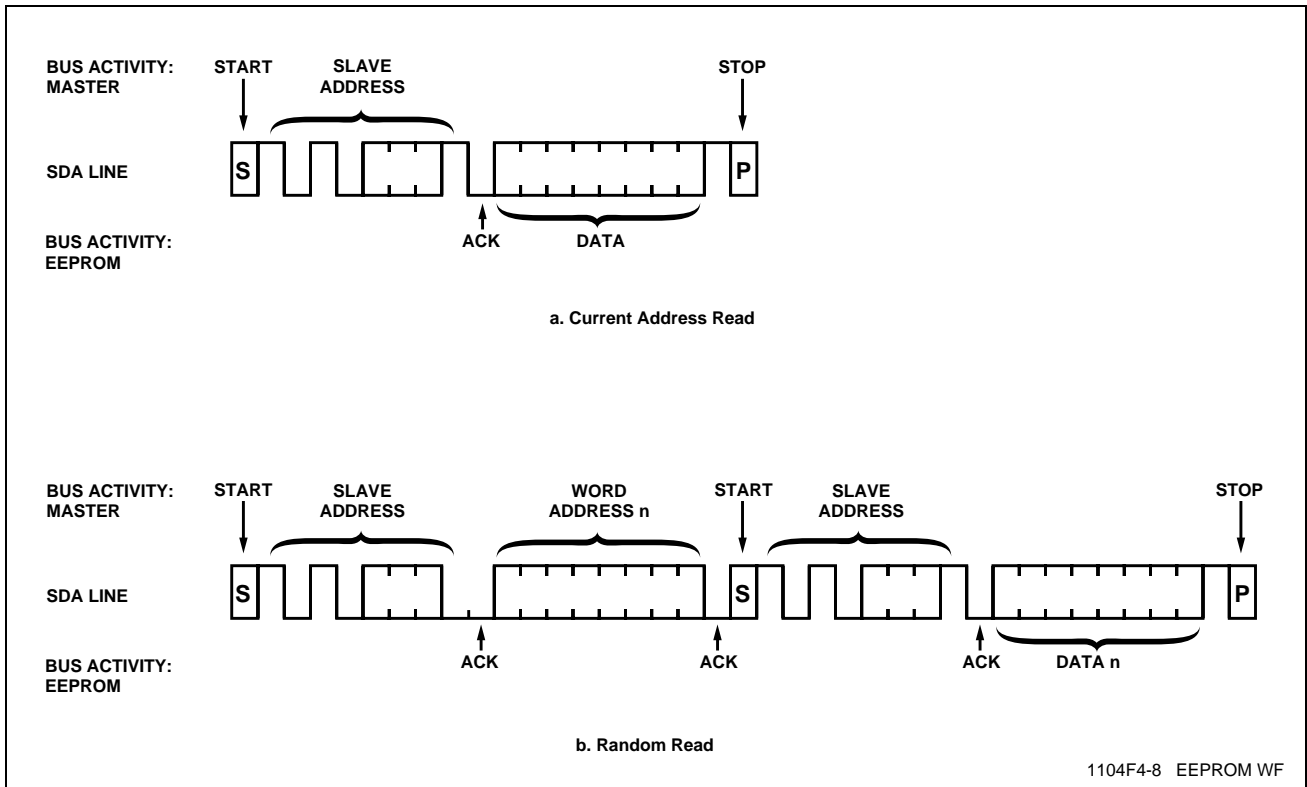
Figure 4-8. Waveforms and Timing – Serial EEPROM Interface

4.3 MIDI Serial Interface Timing

The MIDI interface waveforms and timing is shown in Figure 4-9.
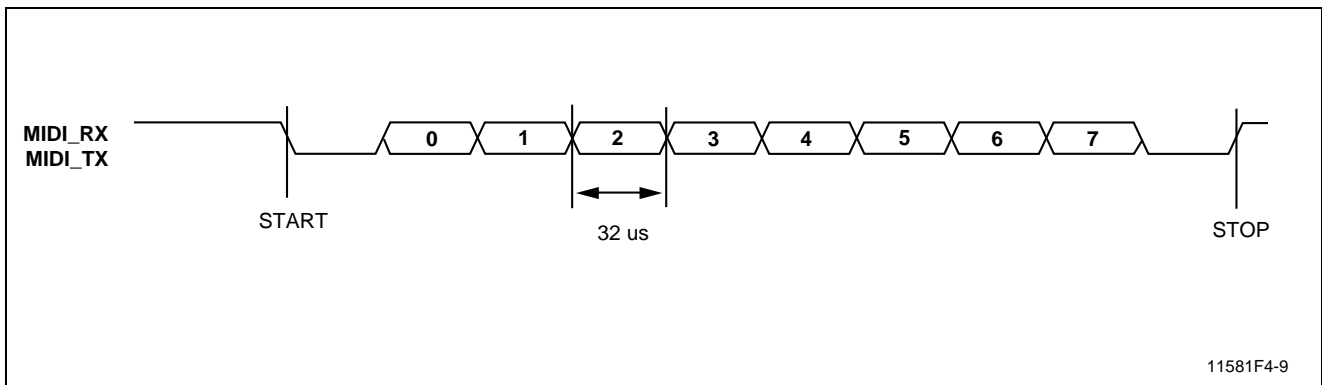
Figure 4-9. Waveforms and Timing – MIDI Interface

5. HOST BUS SOFTWARE INTERFACE

This section describes, from the orientation of the PC, the ISA Bus interfaces and their relative functions,. These interfaces are categorized according to the registers shown in Table 5-1 for Sound Blaster Pro, MPU-401, FM (OPL3), and WaveArtist. Each category is described as a separate section within this document.

5.1 ISA Bus Interface Register Map

Table 5-1. ISA Bus Interface Register Map

Address (Hex)	Bits	W/R	Function
201	8	W/R	Game Port
SB+0, SB+8, 388	8	W	Music 0 Address
SB+0, SB+8, 388	8	R	Music 0 Status
SB+1, SB+9, 389	8	W	Music 0 Data
SB+2, SB+8, 38A	8	W	Music 1 Address
SB+3, SB+8, 38B	8	W	Music 1 Data
SB+4	8	W	Sound Blaster Mixer Address
SB+5	8	W/R	Sound Blaster Mixer Data
SB+6	8	W	Sound Blaster Reset
SB+A	8	R	Sound Blaster Data
SB+C	8	W	Sound Blaster Data
SB+C	8	R	Sound Blaster Write Status
SB+E	8	R	Sound Blaster Read Status
MB+0	8	W/ R	MPU 401 Data Register
MB+1	8	W	MPU 401 Command Register
MB+1	8	R	MPU 401 Status Register
WB+0, 1	16	W/R	WaveArtist Command Register Low Byte
		W/R	WaveArtist Command Register High Byte
WB+2, 3	16	W/R	WaveArtist Data Register Low Byte
		W/R	WaveArtist Data Register High Byte
WB+4	8	W/R	WaveArtist Control Register (CTRLR)
WB+5	8	R	WaveArtist Status Register (STATR)
WB+6	8	W/R	WaveArtist Expansion Control Register 1
WB+7	8	W/R	WaveArtist Expansion Control Register 2
WB+8,9	16	W/R	WaveArtist Expansion Data Register 1
WB+A,B	16	W/R	WaveArtist Expansion Data Register 2
3F8-3FF		W/R	Communications Port 1 (COM1)
2F8-2FF		W/R	Communications Port 2 (COM2)
3E8-3EF		W/R	Communications Port 3 (COM3)
2E8-2EF		W/R	Communications Port 4 (COM4)

Notes:

SB = Sound Blaster Pro interface base register (typically 220 or 240 as assigned by PnP setup).

MB = MPU-401 interface base register (typically 300 or 330 as assigned by PnP setup).

WB = WaveArtist interface base register (typically between 0250 and 03F0 as assigned by PnP setup).

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6. PLUG-AND-PLAY INTERFACE

The PnP interface is supported with 6 logical devices. IRQ3 , 4, 5, 7, 9, 10, 11, 15, DMA 1, 5, 6, 7 and programmable IO base address assignments are available for the 6 logical devices. Address assignment, IRQ, DRQ, and DACK signal routing are done via software driver writing to configuration registers after successful PnP isolation. See ISA Plug-and-Play specification.

6.1 PnP Resource Data

An example of PnP resource data is shown below.

Address (Dec.)	Data (Dec.)	Data (Hex.)	Description
1	4A	74	Vendor ID Name :
2	73	115	RSS
3	50	80	Vendor ID Product Number : 5000
4	00	0	
5	01	1	Serial Number: 00000001
6	00	0	
7	00	0	
8	00	0	
9	69	105	Checksum (LFSR)
10	0A	10	PnP Version and Card String ID
11	10	16	PnP Ver 1.0
12	00	0	Rockwell ver 0
13	82	130	Identifier string ANSI
14	13	19	LSB length
15	00	0	MSB length
16	52	82	R
17	6F	111	o
18	63	99	c
19	6B	107	k
20	77	119	w
21	65	101	e
22	6C	108	l
23	6C	108	l
24	20	32	
25	57	87	W
26	61	97	a
27	76	118	v
28	65	101	e
29	41	65	A
30	72	114	r
31	74	116	t
32	69	105	i
33	73	115	s
34	74	116	t
35	15	21	Logical Device ID
36	4A	74	Logical Device ID 0 Wave Artist Wave Audio
37	73	115	
38	50	80	RSS 5000
39	00	0	
40	02	2	IO Range Check Enabled Reg 31 No boot
41	30	48	Dependent Function Tag
42	47	71	I/O Port Descriptor
43	01	1	16 bit address decode
44	50	80	Min base low
45	02	2	Min base high (0250)
46	F0	240	Max base low
47	03	3	Max base high (03F0)
48	10	16	Alignment for min base address
49	10	16	Range length
50	2A	42	DMA Format
51	E0	224	Channel 5 or 6 or 7
52	12	18	16 bit, count by word

53	38	56	End Dependent Function Tag
54	15	21	Logical Device ID
55	4A	74	Logical Device ID 1 Sound Blaster
56	73	115	
57	50	80	RSS 5001
58	01	1	
59	02	2	IO Range Check Enabled Reg 31 No boot
60	30	48	Dependent Function Tag
61	2A	42	DMA Format
62	02	2	Channel 1
63	08	8	8 bit, count by byte
64	47	71	I/O Port Descriptor
65	01	1	16 bit address decode
66	20	32	Min base low
67	02	2	Min base high (0220)
68	40	64	Max base low
69	02	2	Max base high (0240)
70	20	32	Alignment for min base address
71	10	16	Range length
72	47	71	I/O Port Descriptor
73	01	1	16 bit address decode
74	88	136	Min base low
75	03	3	Min base high (0388)
76	88	136	Max base low
77	03	3	Max base high (0388)
78	04	4	Alignment for min base address
79	04	4	Range length
80	22	34	IRQ Format
81	A0	160	IRQ 5 or 7 or 10
82	04	4	
83	38	56	End Dependent Function Tag
84	15	21	Logical Device ID
85	4A	74	Logical Device ID 2 MPU401
86	73	115	
87	50	80	RSS 5002
88	02	2	
89	02	2	IO Range Check Enabled Reg 31 No boot
90	31	49	Dependent Function Tag
91	00	0	Preferred Configuration
92	47	71	I/O Port Descriptor
93	01	1	16 bit address decode address 330
94	30	48	Min base low
95	03	3	Min base high (0330)
96	30	48	Max base low
97	03	3	Max base high (0330)
98	04	4	Alignment for min base address
99	04	4	Range length
100	22	34	IRQ Format
101	A0	160	IRQ 5 or 7
102	8C	140	or IRQ 10 or 11 or 15
103	31	49	Dependent Function Tag
104	01	1	Acceptable Configuration
105	47	71	I/O Port Descriptor
106	01	1	16 bit address decode address
107	00	0	Min base low
108	03	3	Min base high (0300)
109	00	0	Max base low
110	03	3	Max base high (0300)
111	04	4	Alignment for min base address
112	04	4	Range length
113	22	34	IRQ Format
114	A0	160	IRQ 5 or 7
115	8C	140	or IRQ 10 or 11 or 15
116	31	49	Dependent Function Tag
117	02	2	Suboptimal Configuration
118	47	71	I/O Port Descriptor
119	01	1	16 bit address decode address

120	00	0	Min base low
121	03	3	Min base high (0300)
122	30	48	Max base low
123	03	3	Max base high (0330)
124	30	48	Alignment for min base address
125	04	4	Range length
126	22	34	IRQ Format
127	A0	160	IRQ 5 or 7
128	8E	142	or IRQ 9 or 10 or 11 or 15
129	38	56	End Dependent Function Tag
130	15	21	Logical Device ID
131	4A	74	Logical Device ID 3 Modem
132	73	115	RC288ACF/SP
133	01	1	RSS 0160
134	60	96	
135	02	2	IO Range Check Enabled Reg 31 No boot
136	1C	28	Compatible device ID:PNPC11E
137	41	65	
138	D0	208	
139	C1	193	
140	1E	30	
141	31	49	Dependent Function Tag COM3 more IRQ
142	00	0	Most preferred
143	47	71	I/O Port Descriptor
144	01	1	16 bit address decode
145	E8	232	Min base low
146	03	3	Min base high (03E8)
147	E8	232	Max base low
148	03	3	Max base high (03E8)
149	08	8	Alignment for min base address
150	08	8	Range length
151	22	34	IRQ Format
152	A0	160	IRQ 5,7,10,11,15
153	8C	140	
154	31	49	Dependent Function Tag COM4 more IRQ
155	00	0	Most preferred
156	47	71	I/O Port Descriptor
157	01	1	16 bit address decode
158	E8	232	Min base low
159	02	2	Min base high (02E8)
160	E8	232	Max base low
161	02	2	Max base high (02E8)
162	08	8	Alignment for min base address
163	08	8	Range length
164	22	34	IRQ Format
165	A0	160	IRQ 5,7,10,11,15
166	8C	140	
167	31	49	Dependent Function Tag COM1
168	01	1	Acceptable
169	47	71	I/O Port Descriptor
170	01	1	16 bit address decode
171	F8	248	Min base low
172	03	3	Min base high (03F8)
173	F8	248	Max base low
174	03	3	Max base high (03F8)
175	08	8	Alignment for min base address
176	08	8	Range length
177	22	34	IRQ Format
178	B0	176	IRQ 4,5,7,10,11,15
179	8C	140	
180	31	49	Dependent Function Tag COM2
181	01	1	Acceptable
182	47	71	I/O Port Descriptor
183	01	1	16 bit address decode
184	F8	248	Min base low
185	02	2	Min base high (02F8)

186	F8	248	Max base low
187	02	2	Max base high (02F8)
188	08	8	Alignment for min base address
189	08	8	Range length
190	22	34	IRQ Format
191	A8	168	IRQ 3,5,7,10,11,15
192	8C	140	
193	31	49	Dependent Function Tag COM3
194	01	1	Acceptable
195	47	71	I/O Port Descriptor
196	01	1	16 bit address decode
197	E8	232	Min base low
198	03	3	Min base high (03E8)
199	E8	232	Max base low
200	03	3	Max base high (03E8)
201	08	8	Alignment for min base address
202	08	8	Range length
203	22	34	IRQ Format
204	B0	176	IRQ 4,5,7,10,11,15
205	8C	140	
206	31	49	Dependent Function Tag COM4
207	01	1	Acceptable
208	47	71	I/O Port Descriptor
209	01	1	16 bit address decode
210	E8	232	Min base low
211	02	2	Min base high (02E8)
212	E8	232	Max base low
213	02	2	Max base high (02E8)
214	08	8	Alignment for min base address
215	08	8	Range length
216	22	34	IRQ Format
217	A8	168	IRQ 3,5,7,10,11,15
218	8C	140	
219	38	56	End Dependent Function Tag
220	15	21	Logical Device ID
221	4A	74	Logical Device ID 4 CD-ROM
222	73	115	Dummy placer with no resource requested
223	50	80	RSS 5003
224	03	3	
225	00	0	No IO Range Check Enabled Reg 31 No boot
226	30	48	Dependent Function Tag No real resources
227	22	34	IRQ Format
228	00	0	
229	00	0	No IRQ
230	38	56	End Dependent Function Tag
231	15	21	Logical Device ID
232	4A	74	Logical Device ID 5 Game Port
233	73	115	
234	50	80	RSS 5004
235	04	4	
236	02	2	IO Range Check Enabled Reg 31 No boot
237	47	71	I/O Port Descriptor
238	01	1	16 bit address decode
239	01	1	Min base low
240	02	2	Min base high (0201)
241	01	1	Max base low
242	02	2	Max base high (0201)
243	01	1	Alignment for min base address
244	01	1	Range length
245	79	121	End Tag
246	93	13933	Check Sum

7. DESIGN CONSIDERATIONS

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the audio device. This is especially important considering the record/play of analog speech and music audio. Suppression of noise is essential to the proper operation and performance of the audio device and interfacing audio circuits.

Two aspects of noise in an OEM board design containing the audio device must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting audio circuit performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired audio performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

The following guidelines are offered to specifically help achieve stated audio device performance and to minimize EMI generation.

7.1 PC BOARD LAYOUT GUIDELINES

7.1.1 General Principles

1. Provide separate digital and analog sections on the board.
2. Keep digital and analog components and their corresponding traces as separate as possible (25 mil minimum) and confined to defined sections.
3. Keep high speed digital traces as short as possible.
4. Keep sensitive analog traces as short as possible.
5. Provide proper power supply distribution, grounding, and decoupling.
6. Provide separate filtered/regulated analog power supply.
7. Provide separate digital ground, analog ground, and chassis ground (if appropriate) planes.
8. Provide wide traces for power and critical signals.
9. Position interface circuits near the corresponding off-board connectors.

7.1.2 Component Placement

1. From the system circuit schematic,
   a) Identify the digital and analog circuits and their components, as well as external signal and power connections.
   b) Identify the digital, analog, and mixed digital/analog components within their respective circuits.
   c) Note the location of power and signals pins for each device (IC).
2. Roughly position digital and analog circuits on separate sections of the board. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board. Typically, the digital circuits will cover one-half of the board, analog circuits will cover one-half of the board.
3. Once sections have been roughly defined, place the components starting with the connectors and jacks.

    a)   Allow sufficient clearance around connectors and jacks for mating connectors and plugs.

    b)   Allow sufficient clearance around components for power and ground traces.

    c)   Allow sufficient clearance around sockets to allow the use of component extractors.

4.   First, place the mixed analog/digital components (e.g., A/D converter, and D/A converter).

    a)   Orient the components so pins carrying digital signals extend onto the digital section and pins carrying analog signals extend onto the analog section as much as possible.

    b)   Position the components to straddle the border between analog and digital sections.

5.   Place all analog components.

    a)   Place the analog circuitry on the same area of the PCB.

    b)   Place the analog components close to and on the side of board containing the RLINE, LLINE, RAUX1, LAUX1, RAUX2, LAUX2, RMIC, LMIC, MONOIN, and MONOOUT signals.

    c)   Avoid placing noisy components and traces near the RLINE, LLINE, RAUX1, LAUX1, RAUX2, LAUX2, RMIC, LMIC, MONOIN, and MONOOUT lines.

6.   Place active digital components/circuits and decoupling capacitors.

    a)   Place digital components close together in order to minimize signal trace length.

    b)   Place 0.1 µF decoupling (bypass) capacitors close to the pins (usually power and ground) of the IC they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI.

    c)   Place host bus interface components close to the edge connector in accordance with the applicable bus interface standard, e.g., use a 2.5-in maximum trace length for ISA bus.

    d)   Place crystal circuit as close as possible to the audio device

7.   Provide a "connector" component, usually a zero ohm resistor or a ferrite bead at one or more points on the PCB to connect one section's ground to another.

7.1.3 Signal Routing

1.   Route the audio signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The noise source, neutral, and noise sensitive pins are listed in Table 7-1.

2.   Keep digital signals within the digital section and analog signals within the analog section. (Previous placement of isolation traces should prevent these traces from straying outside their respective sections.) Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.

3.   Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.

    a)   Route an analog isolation ground trace, at least 50 mil to 100 mil wide.

    b)   Route a digital isolation ground trace, at least 50 mil to 100 mil wide.

4.   Keep host control signals (e.g., IOR#, IOW#, and RESET) traces at least 10 mil thick (preferably 12 - 15 mil).

5.   Keep analog signal (e.g., RMIC, LMIC, LLINE, and RLINE) traces at least 12 mil thick (preferably 15 mil) and short as possible.

6.   Keep all other signal traces as wide as possible, at least 5 mil (preferably 10 mil).Route the signals between components by the shortest possible path (the components should have been previously placed to allow this).

7.   Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.

8.   Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.

9.   Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.

10. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.

11. Keep all signal traces away from the crystal circuit.

12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

13. Eliminate ground loops, which are unexpected current return paths to the power source.

7.1.4 Power

1. Identify digital power (VDD) and analog power (AVDD) supply connections.

2. Where main power enters the PCB (edge connector or power connector), place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground. These capacitors help to supply current surge demands and prevent those surges from generating noise on the power lines that may affect other circuits.

3. Provide a voltage regulator to supply clean analog power (+5VA) to the AVDD pins.

4. Generally, route all power traces before signal traces.

7.1.5 Ground Planes

1. In a 2-layer design, provide digital and analog ground plane areas in all unused space around and under digital and analog circuit components, respectively, on both sides of the board, and connect them such a manner as to avoid small islands. Connect each ground plane area to like ground plane areas on the same side at several points and to like ground plane areas on the opposite side through the board at several points. Connect all DGND pins to the digital ground plane area and AGND pins to the analog ground plane area. Typically, separate the collective digital ground plane area from the collective analog ground plane area by a fairly straight gap. There should be no inroads of digital ground plane area extending into the analog ground plane area or visa versa.

2. In a 4-layer design, provide separate digital and analog ground planes covering the corresponding digital and analog circuits, respectively. Connect all DGND pins to the digital ground plane and AGND pins to the analog ground plane. Typically, separate the digital ground plane from the analog ground plane by a fairly straight gap.

3. In a design which needs EMI filtering, define an additional "chassis" section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be positioned in this section. Fill the unused space with a chassis ground plane, and connect it to the metal card bracket and any connector shields/grounds.

4. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host bus interface, audio interface, CD-ROM interface, game port/MIDI interface, modem interface, and memory (ROM, DRAM). Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.

5. Connect grounds together at only one point, if possible, using a ferrite bead. Allow other points for grounds to be connected together if necessary for EMI suppression.

6. Keep all ground traces as wide as possible, at least 25 mil to 50 mil.

7. Keep the traces connecting all decoupling capacitors to power and ground at their respective ICs as short and as direct (i.e., not going through vias) as possible.

7.1.6 Crystal Circuit

1. Keep all traces and component leads connected to crystal input and output pins (i.e., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.

2. Where a ground plane is not available, such as in a 2-layer design, tie the crystal capacitors ground paths using separate short traces (as wide as possible) with minimum angles and vias directly to the corresponding device digital ground pin nearest the crystal pins.

3. Connect crystal cases(s) to ground (if applicable).

4. Connect crystal capacitor ground connections directly to GND pin on the audio device. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding GND pin.

Table 7-1. RWA010 Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
RWA010/ RWA011	VDD, GND		3-4, 8-9, 19, 22, 2530-31, 37, 53, 62, 65, 70, 75, 84, 89, 123-124, 135	
	AVDD, AGND			91, 96-96, 101, 107, 109, 121-122,
	Crystal	23-24		
	ISA Bus Interface (RWA010)	17-17, 26, 29, 32-36, 38-53,54-61, 63-64, 66-69, 71-74, 76-83, 85-88,		
	ISA Bus Interface (RWA011)	32-36, 38-53,54-61, 63-64, 66-69, 71-74, 76-83, 85-88,		
	EEPROM		1-2, 144	
	CD-ROM (RWA011)		17,-18, 26-29	
	Game port/MIDI Interface	136-143	10-11	
	Audio Interface	94-114, 97		92-94, 97-100, 102-106, 108, 110-114,
	RWA030 interface	12-14, 16, 20-21116-118,	126	
	Modem interface		5-7	
	Control, device interconnect, no connection		15,90, 115, 119-120, 125, 127-134	

7.2 CRYSTAL/OSCILLATOR SPECIFICATIONS

The specifications and recommended suppliers for the crystal are listed in Table 7-2.

Table 7-2. Crystal Specifications – 50.8032 MHz

Characteristic	Value
Rockwell Part No.	333R45-005
Electrical	
Frequency	50.8032 MHz nom.
Frequency Tolerance	±40 ppm (C_L = 8.5 and 11.5 pF)
Frequency Stability	
vs. Temperature	±45 ppm (0°C to 70°C)
vs. Aging	±15 ppm over 5 years
Oscillation Mode	Third overtone
Calibration Mode	Parallel resonant
Load Capacitance, C_L	10 pF nom.
Shunt Capacitance, C_O	6 pF max.
Series Resistance, R_1	35 Ω max. @ 20 μW Drive Level
Drive Level	100 μW correlation; 500 μW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions	11.05 x 4.65 x 13.46 mm
Mounting	Through Hole
Holder	HC-49/U
Suggested Suppliers	
Dimensions	KDS America, Inc.
Mounting	Toyocom U.S.A., Inc.
Holder	Hy-Q International (USA), Inc.

Notes:

1. Characteristics @ 25°C unless otherwise noted.

2. Supplier Information:

> Hy-Q International (USA), Inc.
> Enlanger, KY
> (606) 283-5000

> KDS America, Inc.
> Fountain Valley, CA
> (714) 557-7833

> Toyocom U.S.A., Inc.
> Costa Mesa, CA
> (714) 668-9081

7.3 PACKAGE DIMENSIONS
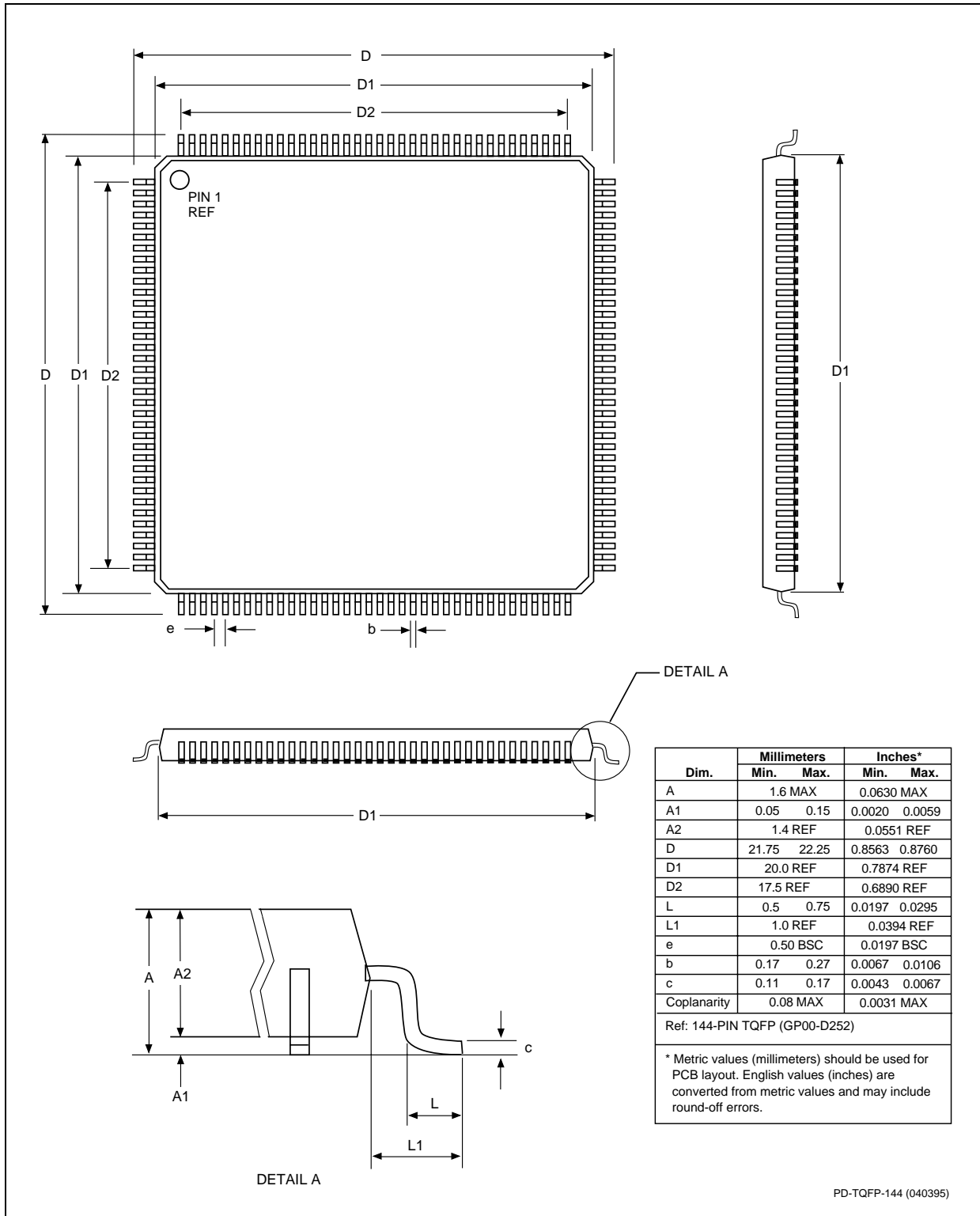
The package dimensions are shown in Figure 7-1.

Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	17.5 REF		0.6890 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-144 (040395)

Figure 7-1. Package Dimensions – 144-Pin TQFP

INSIDE BACK COVER NOTES

REGIONAL SALES OFFICES

Headquarters
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4311 Jamboree Road,
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European Headquarters
Rockwell Semiconductor Systems
S.A.R.L.
Les Taissounieres B1
Route des Dolines
Sophia Antipolis Cedex
06905 Valbonne
France
Phone: (33) 93 00 33 35
Fax: (33) 93 00 33 03

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Suite 103
Richardson, TX 75080
Phone: (214) 379-9310
Fax: (214) 479-9317

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Suite 400
Atlanta, GA 30338
Phone: (770) 393-1830
Fax: (770) 395-1419

US Southeast Satellite Office
Rockwell Semiconductor Systems
Arbor Shoreline Office Park
19345 US 19 N.
Suite 108
Clearwater, FL 34624-3156
Phone: (813) 538-8837
Fax: (813) 531-3031

US Northwest Office
Rockwell Semiconductor Systems
US Northwest Office
3600 Pruneridge Avenue
Suite 100
Santa Clara, CA 95051
Phone: (408) 249-9696
Fax: (408) 249-7113

US North Central Office
Rockwell Semiconductor Systems
Two Pierce Place
Chancellory Park
Suite 810
Itasca, IL 60143
Phone: (708) 773-3454
Fax: (708) 773-3907

US Northeast Office
Rockwell Semiconductor Systems
239 Littleton Road
Suite 4A
Westford, MA 01886
Phone: (508) 692-7660
Fax: (508) 692-8185

Australia
Rockwell Semiconductor Systems
Rockwell Australia Limited
3 Thomas Holt Drive
P.O. Box 165
North Ryde, NSW 2113
Australia
Phone: (61-2) 805 5555
Fax: (61-2) 805 5599

Europe Mediterranean
Rockwell Semiconductor Systems
c/o Rockwell Automation S.r.l.
Via Di Vittorio, 1
20017 Mazzo Di Rho (MI)
Italy
Phone: (39 2) 93179911
Fax   (39 2) 93179913

Europe North
Rockwell Semiconductor Systems, Ltd.
Berkshire Court
Western Road
Bracknell
Berkshire RG12 1RE
England
Phone: +44 1344 486 444
Fax: +44 1344 486 555

Europe South
Rockwell Semiconductor Systems
S.A.R.L.
Tour GAN
Cedex 13
92082 Paris La Defense 2
France
Phone: (33-1) 49-06-3980
Fax: (33-1) 49-06-3990

Germany
Rockwell Semiconductor Systems
Rockwell Int'l GmbH Germany
Paul-Gerhardt-Allee 50 a
81245 Munchen
Germany
Phone: (49-89) 829-1320
Fax: (49-89) 834-2734

Hong Kong
Rockwell Int'l (Asia Pacific) Ltd.
13th Floor, Suites 8-10,
Harbour Centre
25 Harbour Road
Wanchai,
Hong Kong
Phone: (852) 2 827-0181
Fax: (852) 2 827-6488
Phone No: (82.2) 565.2880
Fax No: (82.2) 565.1440

Japan
Rockwell Int'l Japan Co., Ltd.
Shimomoto Bldg
1-46-3 Hatsudai, Shibuya-ku
Tokyo, 151
Japan
Phone: (81-3) 5371 1520
Fax: (81-3) 5371 1501

Korea
Rockwell-Collins Int'l, Inc.
Room No. 1508
Korea Textile Centre Building
944-31, Daechi-3dong
Kangnam P.O. Box 2037
Kangnam-ku
Seoul
Korea
Phone: (82-2) 565-2880
Fax: (82-2) 565-1440

Singapore
Rockwell-Collins Int'l, Inc.
230 Orchard Road #10-230/232
Faber House
Singapore 0923
Phone: (65) 732-2292
Fax: (65) 733-0835

Taiwan
Rockwell Int'l Taiwan Company, Ltd.
Room 2808 International Trade Bldg.
333, Keelung Road, Section I
Taipei,
Taiwan
10548 ROC
Phone: (886-2) 720-0282
Fax: (886-2) 757-6760

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