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Digital Semiconductor 21140A Connection to the Network Using MII-Based Physical Layer Devices:

An Application Note

Order Number: EC–QVQRC–TE

This document provides the information necessary to implement the system and network connections to the Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller. The 21140A is a 10/100-Mb/s Ethernet-to-PCI controller. Other bus implementations can be made through the use of proper bus-to-bus interfaces.

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Contents

Equations

Figures

Tables

1 Implementation Overview

This application note provides a full description of how to implement 100BASE-TX, 100BASE-T4, and 10BASE-T network connections to the Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller (referred to as the 21140A).

The primary objective of this document is to help the user achieve an error-free implementation of the network interface with the 21140A and physical layer (PHY) chips based on the media-independent interface (MII) by using a single network connector. This document provides hardware design and layout recommendations to describe the hardware implementation. In addition, this application note provides design recommendations from PHY device manufacturers. The implementation options described in this application note are supported by the DC21X4 drivers provided by Digital Semiconductor.

This application note does not describe the 21140A software interface. For more information on the software interface, refer to the *Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual*. (See Appendix C for ordering information.)

1.1 Functional Overview

This following sections are an overview of the PCI host system and100-Mb/s and 10-Mb/s network interfaces.

1.1.1 System Interface

The 21140A implements a direct interface to the PCI bus through a single 50-pin connection, which consists of the control and address/data signals. The internal FIFO size of the 21140A eliminates the need for any offchip onboard memory and minimizes CPU utilization through direct memory access (DMA) of the packets to and from host memory.

The bus master design provides for high throughput between the system and the network, while requiring only a minimum number of devices for a complete implementation.

The 21140A performs 33-MHz synchronous DMA cycles when interfacing to the PCI bus. This enables the board to operate while using only 10% of the bus bandwidth during a 100-Mb/s Ethernet reception or transmission.

1.1.2 Network Interface

The 21140A supports the multirate industry-standard MII interface according to the IEEE 802.3u standard. The 21140A provides a dual-rate network interface for both a 100-Mb/s and 10-Mb/s Ethernet through the MII interface. The MII is a nibble-wide (4 bits) standard interface that can be used with various MII-based physical layer network connections such as 100BASE-TX, 100BASE-T4, STP, and fiber.

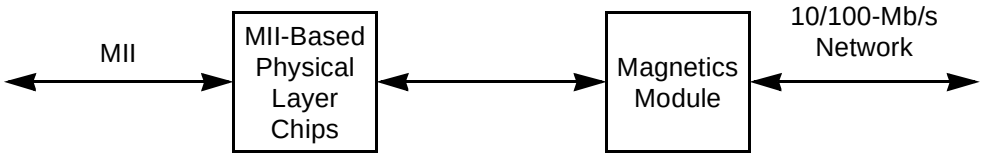
The 10-Mb/s interface can be implemented using the MII port as described in this document, or by using the 7-wire standard connection. For more information on the 7-wire connection refer to the Serial Port section of the *Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual*. (See Appendix C for ordering information).

The 21140A also has a special 100BASE-TX support mode, which is the MII/SYM port. For more information on the MII/SYM port, refer to the MII/SYM Port section in the *Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual*. (See Appendix C for ordering information).

1.2 Block Diagram

Figure 1 is a block diagram of the physical layer design (based on MII physical layer chips) for a 100BASE-T and 10BASE-T single-connector network connection with the 21140A.

Figure 1 Physical Layer Design



The physical layer includes the following:

- The MII-based physical layer chips, which have a direct interface to the MII port of the 21140A with dual-rate option (as specified in the MII specification) and a full interface to the 10/100-Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100-Mb/s network (100BASE-TX or 100BASE-T4) and to the 10-Mb/s network (10BASE-T).

1.3 Power Supply

The 21140A operates with a 3.3-V power supply. For dc conversion, Digital Semiconductor recommends the Linear Technology LT1117 regulator or the Motorola MC33269D regulator. To stabilize the voltage, a 10-µF capacitor and a 47-µF capacitor should be connected across the 5-V input and the 3.3-V output, respectively. To reduce noise, Digital Semiconductor recommends decoupling capacitors (0.1-µF, 0.01-µF, and 10-µF tantalum) for the 21140A supply pins.

1.4 Printed Circuit Board Layout Recommendations

Digital Semiconductor suggests that all of the following recommendations be implemented due to the nature of mixed high speed digital signals and very high speed analog/ECL signals.

1.4.1 PCI Signal Routing

The 21140A complies with the *PCI Local Bus Specification*. Therefore, the pins are arranged in the same order as the edge connector to meet the following PCI requirements for etch line length:

- Up to 1.5 inches between the etch connector and the pads of the 21140A
- Exactly 2.5 inches between the etch connector and the pads of the PCI clock

1.4.2 MII Signal Routing

Because the MII interface passes logic signals at high speed (25 MHz or 2.5 MHz for Ethernet operation), these signals should be routed first, and as directly as possible. Furthermore, these signals should be routed in the external routing layers of the board.

Clock signal termination should be considered for implementations with long trace lines between the 21140A and the MII-based physical layer chip. Specific termination choices (serial, parallel, and so on) should be based on the layout design and simulation analysis.

1.4.3 Ground and Power Planes

A design implemented with the 21140A requires the following two kinds of power signals:

- **Vcc** (5.0 V) driving all the network ENDEC and 21140A external components
- **Vdd** (3.3 V) driving the 21140A chip and a common **gnd** (ground)

To reduce noise, Digital Semiconductor recommends keeping at least two power planes (**Vcc** and **gnd**) on the printed circuit board. The **Vdd** power supply can be supplied through a cut in the **Vcc** power plane or by a power island on one of the signal routing layers underneath the 21140A. In addition, Digital Semiconductor recommends placing all the decoupling capacitors for all power supply pins as close as possible to the power pads of the 21140A.

1.5 Other Considerations

If the JTAG port is not used, the TDO pin (pin 144) should not be connected.

2 National Semiconductor Chipset Implementation

This section contains the design recommendations for the National Semiconductor DP83840 10/100-Mb/s Ethernet Physical Layer (PHY) and DP83223A TWISTER™ High Speed Networking Transceiver (referred to as the DP83840 and DP83223A) in a node application using the 21140A.

2.1 Overview

The DP83840 PHY device incorporates an integrated 10BASE-T transceiver as well as a media-independent interface (MII) for simple connection to the 21140A. The DP83840 is fully compatible with the DP83223A to enable 100BASE-TX compliant signaling.

A design based on these three devices allows for a simple low-cost PCI node design, which will support both 10BASE-T and 100BASE-TX protocols. The comprehensive feature sets of both the 21140A and the DP83840 support several different modes of functionality.

Although design issues such as common magnetics, autonegotiation, and 10/100-Mb/s operation are noted here, detailed emphasis is placed on fundamental design requirements from the MAC to the RJ45-8 connector. Schematic diagrams, layout considerations, and power requirements are all provided in this application note. A magnetics scheme is recommended to help the designer integrate the National Semiconductor parts in a system.

For a given application, the component values and design suggestions in this application note can and will vary with the particular design. This application note illustrates the function of the various components and their relationship to overall system performance. With this knowledge, the system designer can make modifications to the recommendations with an understanding of the potential impact to the system.

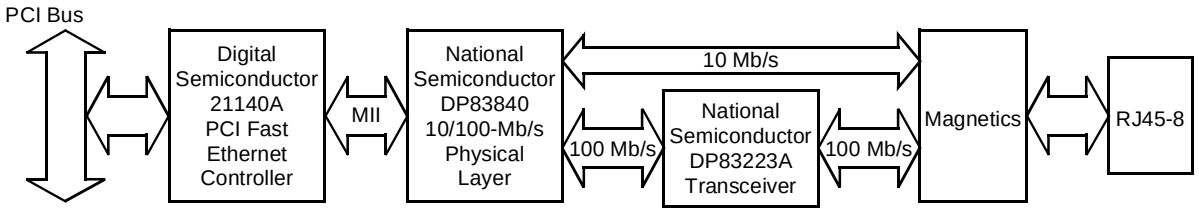
This application note should be reviewed in conjunction with all documentation available on the products covered in this document from both Digital Semiconductor and National Semiconductor. (See Appendix C.)

See Appendix C to order copies of the DP83840 Physical Layer and DP83223A Transceiver data sheets and product samples.

2.2 Block Diagram

Figure 2 is the system diagram for a node application. The following sections describe the blocks; for more detailed information on the specifications of these parts, see the documentation listed in Appendix C.

Figure 2 10/100-Mb/s Block Diagram



2.2.1 DP83840

The DP83840 finds wide application in data communication systems. It is a physical layer device for Ethernet 10BASE-T and 100BASE-X using category 5 (CAT5) unshielded, Type 1 shielded, and fiber-optic cables. It interfaces to the PMD sublayer through a DP83223A and to the MAC layer through the MII, ensuring interoperability between products from different vendors.

The DP83840 system architecture is based on the integration of the following National Semiconductor industry-proven core technologies:

- 10BASE-T ENDEC/ Transceiver module to provide the 10-Mb/s IEEE 802.3 functions
- 100BASE-X physical coding sublayer (PCS) and control logic that integrate the core modules into a dual-speed Ethernet physical layer controller

The DP83840 features include:

- IEEE 802.3 10BASE-T compatibility. ENDEC and UTP/STP transceivers and filters are built in.
- IEEE 802.3u 100BASE-X compatibility with support for category 5 UTP, Type 1 STP, and fiber-optic transceivers. Connects directly to the DP83223A.
- ANSI X3T12 TP-PMD compatibility.
- IEEE 802.3u autonegotiation for automatic speed selection.
- Independent interface (MII) with serial management interface.
- Integrated, high-performance, 100-Mb/s clock recovery circuitry that requires no external filters.
- Full-duplex support for 10 Mb/s and 100 Mb/s.
- MII serial 10-Mb/s output mode.
- Programmable loopback modes for easy system diagnostics.
- Flexible LED support.

2.2.2 DP83223A

The DP83223A twisted-pair transceiver can drive and receive either binary or MLT-3 encoded data streams. The DP83223A allows links of up to 100 meters over both shielded twisted-pair (STP) and data grade unshielded twisted-pair (UTP) or equivalent. The DP83223A also provides important features such as baseline restoration, tristate-capable transmit outputs, and controlled transmit output edge rates (to reduce EMI radiation) for both binary and MLT-3 modes of operation.

The DP83223A features include:

- Integrated baseline restoration circuit
- Integrated transmitter and receiver with adaptive equalization circuit
- Programmable binary or MLT-3 operation
- Isolated TX and RX power supplies for minimum noise coupling
- Controlled transmit output edge rates for reduced EMI
- Tristate capable current transmit outputs
- Loopback feature for board diagnostics
- Programmable transmit voltage amplitude

2.2.3 Magnetics

The magnetics block in Figure 2 uses a common magnetics scheme that allows 10-Mb/s and 100-Mb/s data to coexist in the same magnetics package. The concept of common magnetics is based on the interoperation of the DP83840 and the DP83223A and allows for either 10-Mb/s or 100-Mb/s operation with the use of a single magnetics module and RJ45-8 media connector. (For a complete discussion of the common magnetics concept, refer to the National Semiconductor *10/100 Ethernet Common Magnetics* application note.)

National Semiconductor has patents on the common magnetics scheme, and provides a license to purchasers of both the DP83840 and the DP83223A components with a license to use the common magnetics scheme in their design. National Semiconductor has tested common magnetics modules from various magnetics manufacturers. These devices have been tested for standards compliance with the 10BASE-T and 100BASE-TX specifications. Appendix A contains a list of these magnetics vendors and the license agreement. This is not an exhaustive list and other vendors could be considered, but the transformer would need to be characterized in relation to the *10/100 Base-T Magnetics Specification* (available from National Semiconductor).

2.3 Physical Layer Schematic Diagram Description

Appendix A contains the schematic diagrams for the physical layer. Figure 13 illustrates the interconnection of the DP83840 and DP83223A.

2.3.1 Media-Independent Interface (MII)

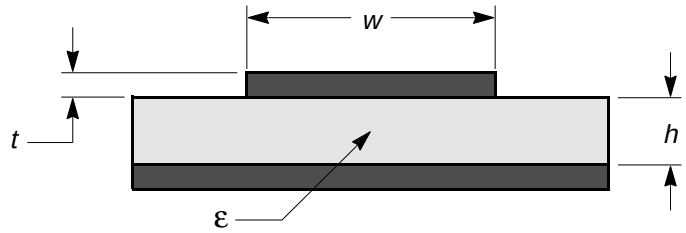
The DP83840 has a standard IEEE 802.3u MII for connection to external 10-Mb/s or 100-Mb/s physical layer devices. This comprises nibble-wide (4-bits) transmit and receive data streams, transmit and receive clocks, transmit enable, receive collision, receive carrier sense, receive data valid, data error, and serial management data clock and data signals. These signals are: TX_CLK, TXD[3:0], TX_EN, CRS, COL, RXD[3:0], RX_CLK, RX_DV, RX_ER, MDC, MDIO, and RSTOUT.

The MII supports two nibble clock rates: 2.5 MHz for 10-Mb/s operation and 25 MHz for 100-Mb/s operation. Operation at 10 Mb/s or 100 Mb/s is transparent to the host.

2.3.2 Signal Terminations

The MII signal lines are: TX_CLK, TXD[3:0], TX_EN, CRS, COL, RXD[3:0], RX_CLK, RX_DV, RX_ER, MDC, MDIO, and RSTOUT. The trace impedance of each MII line should be approximately 68 Ω per the IEEE specification. The design of microstrips for PC boards is straightforward and a function of the microstrip width (w) and thickness (t) and the height (h) and relative electric permittivity of the substrate (ε), as shown in Figure 3.

Figure 3 Microstrip impedance



Equation 1 shows how the various geometric and material parameters on the printed circuit board (PCB) control the impedance of the trace. Most of the PCB programs calculate the trace impedance directly.

Equation 1 Microstrip Impedance

$$Z = \left(\frac{87}{(\varepsilon_r + 1.41)}\right)\ln\left(\frac{5.98h}{(0.8w + t)}\right)$$

The DP83840 supports 10-Mb/s and 100-Mb/s Ethernet using the DP83223A and the common magnetics approach. The following signal lines between the DP83840 and the DP83223A should be PECL (Thevenin) terminated at the DP83223A: PMRD+, PMRD–, PMID+, PMID–, SD+, and SD–. These signal lines are Thevenin terminated (see Figure 15) with an equivalent resistance equal to the trace impedance. This trace impedance should be controlled and match the device termination resistance. For the preferred case of a 50-Ω transmission interconnect, resistors R23 through R28 are 82.5 Ω to **Vcc** and R6 through R9, R21, and R22 are 130 Ω to ground. This generates a 50.3-Ω Thevenin resistance. The trace impedance of these signal lines should also be 50 Ω.

It is critical that these lines be kept short (<1 inch) and that the termination resistors are as close as possible to the destination. If the PECL termination resistors are not placed close to the signal destination, reflections might result and could corrupt the signal integrity. The mid-level voltage of the termination network should be 3.0 V and the required bias current is 23.5 mA due to each line termination.

The 50-Ω termination is the most robust approach, requiring 23.5 mA per PECL termination. In this application there are six terminations totaling 141 mA. This might be excessive current draw for certain applications and higher values of termination resistance could be considered. For example, in the *Unmanaged Repeater* application note, the termination values are 160 Ω to **Vcc** and 260 Ω to ground. This is a 100-Ω Thevenin resistance and the current draw is reduced to 11.75 mA per termination. A reasonable upper bound might be a Thevenin resistance of approximately 100 Ω to 200 Ω. To ensure that the data maintains integrity as the resistor values increase, check the quality of the high-speed interconnect signal with an oscilloscope, looking for minimal ringing and equal rise and fall times in the waveform.

In Fast Ethernet systems, special attention needs to be given to transmission type effects. If proper line termination is not used for a given application, ringing will occur on these lines. It is worth noting that the SD± signal detect lines are detecting either the presence of a valid signal on the RXI± inputs or that loopback mode has been selected. In either case, low-speed and higher value termination resistors can be used.

2.3.2.1 Signal Transmission

When the 100-Mb/s port is enabled, the DP83223A TXO± outputs are directly connected across the entire primary of the common magnetics transmit section of the transformer. Because this connection uses a 1:1 isolation transformer, the 2-V peak-to-peak (5%), differential MLT-3 signal generated by the DP83223A is maintained as it is coupled onto the UTP. The 100-Mb/s operation uses the transmit transformer in a unity gain configuration (less the insertion loss). The source termination resistance is established by the sum of R4 and R5 (47.5 Ω × 2), and the ON resistance of the solid-state switches Q3 and Q4 (2.5 Ω × 2), as shown in Figure 16. This circuit resistance should be equal to the cable impedance of 100 Ω or 150 Ω for UTP or STP.

The DP83840 TXU± output provides standard 10BASE-T signaling, as shown in Figures 14 and 15 and Figure 2 of the *10/100 Ethernet Common Magnetics* application note. This differential signal is coupled to one-half of the transmit isolation transformer primary winding through series resistors R1 and R2 and capacitors C32 and C30. Equation 2 shows the basic transformer equations.

Equation 2 Transformer Equations

A. $$\frac{V_p}{V_s} = \frac{n_p}{n_s} = N$$

B. $$Z_p = N^2 Z_s$$

Equation 2A is the turns ratio as a function of the secondary and primary voltages, and Equation 2B is the primary impedance as a function of the secondary load and turns ratio (N). In Equation 2, subscripts *p* and *s* represent primary and secondary, *V* represents voltage, and *Z* represents impedance.

In 10BASE-T transmit mode, the turns ratio (n_p/n_s) is 1/2. The secondary load impedance for UTP cable is 100 Ω. For the primary impedance to match the secondary impedance, a primary impedance of 25 Ω is required. This scales through the transformer voltage gain to appear as 100 Ω. This primary impedance is established by resistors R1 and R2 (10.5 Ω each) and the output impedance of the driver ports TXU± (2 Ω each) (see Figure 15). The series sum of these resistances is 25 Ω.

Good signal transfer is maintained by matching the cable impedance to the driving impedance. Resistor R3 and capacitors C1 and C8 are included to provide a balanced impedance across each leg of the transmit transformer primary winding and high-frequency rolloff, which improves FCC characteristics.

Bypass capacitors C29 to C32 and C8 have been added since the initial work on the 10/100 common magnetics. These capacitors compensate for the rising output impedance of the 10-Mb/s transmit driver circuits. This circuit establishes a pole-zero pair, with the zero being at approximately 15 MHz. Placing the zero at 15 MHz balances the increasing output impedance term. The effect of adding these capacitors is a 2-dB to
3-dB improvement in transmit return loss measurement. These capacitors should be added to existing and new designs if possible.

2.3.2.2 Signal Receive Operation

As shown in Figure 13 and Figure 3 of the *10/100 Ethernet Common Magnetics* application note, the 100-Mb/s receive signal is coupled from the cable by an isolation transformer with a 1:1 turns ratio. The DP83223A RXI± inputs receive the 100-Mb/s data through the attenuation network comprising resistors R29 through R32 and capacitor C14. This attenuation network is required to optimize the adaptive equalization function within the DP83223A receiver. A recent application note, *DP83223 TWISTER Adaptive Equalization Considerations*, discusses the attenuation network details and component selection.

A particular system design must take into account the actual amount of transformer insertion loss. This measured value of insertion loss and the manufacturer-specified tolerances can be used to determine the correct resistor divider ratio for the network attenuator. It is critical that the overall attenuation resistance be maintained at 100 Ω (series resistance of R29 through R32). The attenuation circuit (shown in Figure 15) comprises two series 12-Ω resistors (R31 and R32), which provide a 24-Ω differential impedance to the incoming signal. Additionally, R29 and R30 form a 76-Ω combination that, when combined with the 24-Ω series resistance, creates the required 100-Ω forward cable termination. The attenuation network resistors should have a tolerance of 0.5% to maintain signal tolerance. The DP83223A RXI± inputs receive the signal as it appears across the attenuator voltage divider. This attenuated voltage should be 1.45 V ±10%. Measurements should be made on the system to ensure that the correct voltage is being received. This method of measurement is described in the *DP83223 TWISTER Adaptive Equalization Considerations* application note.

Capacitor C14 (0.01 µF) is placed at the center point of the attenuation resistors. This capacitor provides common-mode ground reference, reducing system sensitivity to common-mode noise.

Note: The selection of the attenuation network components is extremely critical for good system performance. Refer to the *DP83223 TWISTER Adaptive Equalization Considerations* application note for the detailed design of this circuit.

An isolation transformer with a 1:1 turns ratio couples the 10-Mb/s differential receive signal from the cable. This differential signal is capacitively coupled through C9 and C10 to the DP83840 RXI± inputs (see Figure 14). Because the signals are capacitively coupled to the DP83840 RXI± high-impedance inputs, dc current is blocked, ensuring signal levels with the proper common-mode voltage as set by the DP83840. In addition to the Manchester encoded 10BASE-T data, the DP83840 RXI± inputs receive normal link pulses and fast link pulses to allow Nway autonegotiation functionality.

2.3.3 STP Operation

The DP83840 can be configured, through internal control register access, to source data through the TXS± outputs for shielded twisted-pair operation. In this case, the unshielded TXU± outputs are tristated to eliminate contention. Similarly, the TXS± outputs are tristated during 10-Mb/s unshielded twisted-pair signaling from TXU±. Other than resistor and capacitor value changes to accommodate 150-Ω STP cable, all remaining interaction between the DP83840 and the DP83223A remain as stated in

Sections 2.3.1 through 2.3.3. Additionally, the RJ45-8 modular jack used for unshielded twisted-pair applications is replaced by a media connector (DB-9). Refer to Section 2.3.5 for the connection information.

Table 1 Component Values Required for STP or UTP Operation

Configuration	R3	C8 (pF)	C1 (pF)	R10	R4	R5	R16 R17	R1 R2	C29/C31 (pF)	C30/C32 (pF)	R31 R32	R29 R30
UTP	12.4	820	18	511	47.5	47.5	×	10.5	×	1000	12	38
STP	16.5	620	18	625	73	73	16.5	×	620	×	29	46
STP & UTP Connected	7.5	1400	36	*	*	*	*	*	*	*	*	*

× = Do not install component.

2.3.4 Common-Mode Termination

The intent of common-mode termination is to help reduce unwanted contributions to EMI emissions and susceptibility by properly terminating the common-mode energy that can exist on the twisted-pair cable. This technique is designed for unshielded twisted-pair applications that, due to the lack of a shield, inherently possess high susceptibility to common-mode noise sources.

2.3.4.1 Transmit Active Pair Termination

Figure 16 and the *10/100 Base-T Magnetics* specification suggest the use of a center-tapped transformer within the transmit magnetics. This allows access to the common-mode signal present on the cable. The impedance of the common-mode channel within an unshielded twisted-pair can be calculated to be approximately 75 Ω. To obtain the 75-Ω common-mode resistance, R18 (50 Ω) is connected between the transformer center-tap and capacitor C5 (500 pF to 1000 pF @ 2 kV rms). This resistance, when combined with the cable differential termination resistance, provides 75 Ω. The other side of C5 is connected to chassis ground. This capacitor requires a 2 kV rms rating to guard against high energy transients coupled onto the LAN cable systems and static charge buildup on LAN cables and components. The *TP-PMD* specification (Sections 8.4 to 8.4.2.2, Isolation Requirements) establishes the voltage rating for the capacitor. The inclusion of this capacitor also improves circuit performance, providing a solid common-mode reference and reducing common-mode noise.

The high voltage capacitor can be fabricated using the printed circuit board as the dielectric. The capacitor should be designed onto the chassis side of the board, using all four layers to get the required capacitance (see Section 2.5.2). Equation 3 is the equation for a parallel plate capacitor.

Equation 3 Parallel Plate Capacitance

$$C = 8.85\left(\frac{\varepsilon_r A}{l}\right)$$

C is in pF, A is the area of the plates in m^2, l is the separation of the plates in m, and ε_r is the relative permittivity of the medium between capacitor plates.

Dielectric strength (DS) is a critical parameter of this capacitor. This is the voltage that can be placed across the part prior to breakdown. For a given plate spacing this breakdown is proportional to the dielectric strength of the medium between the plates. The radius of curvature of the edge of the capacitor plate is another factor. With the printed circuit board as the medium (which is essentially epoxy/fiberglass), the DS is 400 V/mil. For a standard 4-layer board with an overall thickness of 0.062 in, the dielectric strength is approximately 6400 V between capacitor plates.

2.3.4.2 Receive Active Pair Termination

Figure 16 shows R57 (50 Ω) connected to the center-tap of the receive transformer primary to provide a common-mode attenuation connection point.

2.3.4.3 Unused Pair Termination

Unused pairs 4-5 and 7-8 are tied together and connected to the same 2 kV rms capacitor (C5) through two 75-Ω resistors (R19 and R20). This provides direct termination for potential common-mode noise on the unused pairs. Because of cross talk, common-mode noise present on the unused pairs can also be detrimental.

2.3.5 Media Connections

Tables 2 and 3 show the pinout requirements for UTP and STP node connections.

Table 2 Unshielded Twisted-Pair RJ45-8 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	1 (TX+) and 2 (TX–)
Receive pair	3 (RX+) and 6 (RX–)
Unused pair	4 and 5
Unused pair	7 and 8

Table 3 Shielded Twisted-Pair DB-9 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	5 (TX+) and 9 (TX–)
Receive pair	1 (RX+) and 6 (RX–)
Unused pins	2, 3, 4, 7, and 8
Ground to chassis	Shield

2.4 Layout Considerations

The goal of any complex system design, especially one that includes both analog and digital functionality, is to achieve the most robust system performance possible. Performance aspects such as bit-error-rate, EMI, and general signal integrity must be considered.

The correct combination of component placement, signal routing practices, and power supply distribution will yield a robust and reliable system.

This section considers the physical design aspects of a 10/100 Ethernet system design using National Semiconductor physical layer devices in conjunction with common magnetics. The National Semiconductor *1996 National Ethernet Databook* discusses the theory and practice of system design. The *Transmission Line Concepts* and *System Considerations* application notes provide excellent guidelines.

2.4.1 Component Placement

The relative placement of the active and passive components within a system design is essentially defined by important design parameters, such as performance, cost, and board area.

Figure 4 shows a potential component layout that will yield good signal integrity and good overall performance. The layout minimizes the required board area while optimizing the relative component placement.

The layout of the dynamic transmit and receive signals at the twisted-pair transceiver interface is critical to good performance. As shown in Figure 4, the DP83840 is orientated such that its TD, RD, and SD signal pins are in close proximity to the PMRD, SD and PMID signals on the DP83223A. These signals carry the transmit and receive 100-Mb/s data and their length should be minimal. This configuration shows the MII connector adjacent to the DP83840 pins that contain the MII signals (pins 51-80). The oscillator is adjacent to the OSC_IN pin on the DP83840. Keeping the oscillator close to the device minimizes jitter at the clock output. Clearly, component location can vary depending on the other devices being used in the application.

Note: In the system layout it is critical to maintain short distances between the transmit and receive sections of the DP83840 and DP83223A and to place the MII adjacent to the DP83840 (pins 51-80).

2.5 Special Considerations

Incorporate controlled impedance routing for the signal traces that carry the 125-Mb/s serial bit stream. Standard microstrip or stripline techniques are recommended. Choose an impedance of 50 Ω for each trace that transports the 125-Mb/s information between the RJ45-8, common magnetics, and the DP83223A transceiver. This is required to match the 100-Ω differential impedance of the unshielded twisted-pair cable.

The 125-Mb/s PECL signals connected between the DP83223A and the DP83840 can be designed as 50-Ω to 100-Ω impedance traces. The choice of PECL terminating resistors will determine the trace impedance, such that they are consistent with each other.

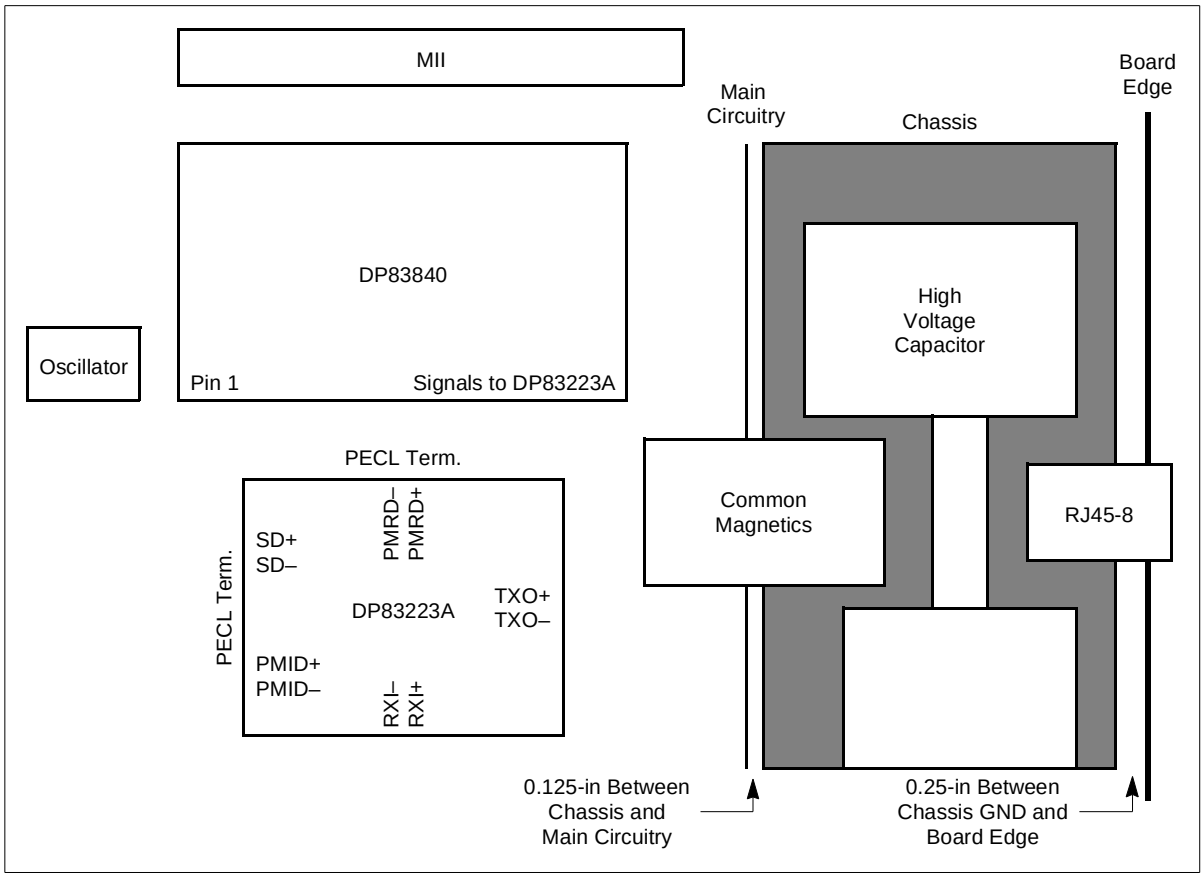
2.5.1 General Guidelines

General guidelines regarding optimal signal trace routing practices include:

- Minimal length, controlled-impedance signal traces to minimize reflections and decrease noise sensitivities. The most critical signals are between the DP83840 and the DP83223A and the signals from the RJ45-8 to the transformer. The signal traces from the RJ45-8 to the transformer should be stripline with an impedance of 50 Ω.
- Matched length differential signal traces to minimize jitter.

- Radiused, routed trace corners of >45°.
- Minimum number of vias for a given signal trace to minimize radiation.
- ECL terminations placed close to signal destination.
- All controlled impedance traces routed directly over or under uninterrupted power or ground planes on adjacent layers. This minimizes noise coupled into signal lines.

Figure 4 Physical Layer Component Placement Recommendation



2.5.2 Board Layers

The number of board layers will vary depending on the signal routing density. In general, a 4- to 6-layer design is sufficient. The 4-layer case shown in Figure 4 is sufficient for most node applications.

Figure 5 shows one potential option for PCB layer assignment, a configuration with good FCC results. Layers 1 and 4 are for signal routing, layer 2 is the ground plane, and layer 3 is **Vcc** for the circuit devices. On the chassis side of the card, layer 1 is chassis ground, layer 2 is for signals and capacitor, layer 3 is chassis ground, and layer 4 is the capacitor plate. For the capacitor, layer 2 is connected to 4 (as one plate) and layers 1 and 3 are the ground side of the capacitor. Configuring the capacitor in this way has the net effect of three capacitors in parallel.

Figure 5 Board Layer Recommendation.

	Main Circuitry	Chassis Side
1	Signals	Chassis GND
2	GND	Signals
3	Power	Chassis GND
4	Signals	Capacitor Plate

2.5.3 Ground Plane Partitioning

Recent system measurements at National Semiconductor show that the single ground plane approach is one way to minimize EMI. Ground-plane partitioning can cause increased EMI emissions that might make the system noncompliant with specific FCC regulations. Figure 4 shows a recommended ground layout scheme and specifies the placement and space between the system ground and chassis ground.

Keeping the chassis ground approximately 0.25-inches from the edge of the system motherboard and voiding that gap of any copper will help to reduce any potential fringe radiation that might occur during system operation. This is permissible because no active traces need to be routed in this area.

2.6 Power Requirements

Careful power supply filtering and isolation practices can provide a minimal noise environment for each of the unique digital and analog sections of the DP83223A and DP83840. A recommendation is to use one power and one ground plane. Recent system measurements made at National Semiconductor on a 10/100 Ethernet system showed reduced (approximately 7 dB) EMI emissions in single ground and **Vcc** plane systems as compared to multiple **Vcc** and ground islands interconnected by ferrite beads.

As the data rates begin to increase, power and ground plane partitioning require careful consideration. To be compliant with electrical isolation issues, the chassis ground needs to be physically isolated from the system circuit ground. The dc voltage for the circuit card should be derived from a stable power supply. The power supply input decoupling circuit should provide enough capacitance to keep the supply at full voltage and additional bypassing to maintain low impedances at high frequencies. Typically, a capacitor to keep the voltage stable (10 µF) and a high frequency bypass capacitor (0.01 µF) are sufficient for the card if the supply is stable and clean. Careful attention to power decoupling is required on the physical layer devices and is described in Section 2.6.1.

2.6.1 DP83840 and DP83223A Decoupling

The DP83840 internally partitions the power sections into four basic groups: PLL, analog (ANA), RX/TX, and digital. To maintain the integrity of these power partitions PLL, TX/RX, ANA, and digital power pins are decoupled as shown in Figure 14. The schematic shows a typical connection with parallel 10-µF and 0.01-µF capacitors and a series inductor (C24, C4, and L3 [Murata BLM31A02]) to the **Vcc** power plane. This allows for the attenuation of low and high frequency noise. For the PLL and ANA **Vcc,** a series resistor can be added to provide further isolation. The value of this resistor should be < 4 Ω to keep the voltage drop low.

In certain applications it might be possible to simplify the decoupling circuit on these pins. The best way to ascertain if this is the case is to measure the power supply noise using a spectrum analyzer on the power input and at the device pin. If this value is not influenced by the decoupling circuit, it might be possible to simplify the circuit. The present scheme provides good isolation, filtering, and voltage stability. For local decoupling on the DP83223A, connect RX and TX together with a large pad and use 10-µF and 0.01-µF capacitors in parallel and a series inductor to the power plane. Figures 14 and 15 show the details of chip decoupling.

2.7 Recommended Parts List for Physical Layer

Table 4 lists the recommended parts for the physical layer.

Table 4 Recommended Parts List for Physical Layer *(Sheet 1 of 2)*

Description	Value	Volts	Tolerance	Package	Qty	Reference
C/CER	18 pF	50	10%	SMD0805	1	C1
C/CER	27 pF	50	10%	SMD0805	1	C35
C/CER	620 pF	50	10%	SMD0805	2	C29, C31
C/CER	1000 pF	50	+80-20%	SMD1206	2	C30, C32
C/CER	0.01 µF	50	+80-20%	SMD1206	14	C2, C6, C11-C18, C22-C25
C/CER	820 pF	50	10%	SMD1206	1	C8
C/CER	0.1 µF	50	+80-20%	SMD1206	2	C9, C10
C/CER	500-1000 pF	2 kV rms	20%	Through-hole	1	C5
Polarized capacitor	10 µF	16	20%	SMD	9	C3, C4, C7, C19-C21, C26, C28, C36
Inductor	—	—	—	SMT	3	L1, L3, L5
Telco connector	—	—	—	TH	1	J2
MII 100-Mb connector	—	—	—	RT/A_PCB_CONN	1	J1
Oscillator 50 MHz	—	—	—	Half-size	1	Y3
LED	Green	—	—	LED-dial 5-50 typ05	5	D2-D6
LED	Green	—	—	LED-pcb-mtra	1	D1
Resistor	4.7 kΩ	—	5%	r500	1	R63
Resistor	10.5 Ω	—	1%	1206	1	R3
Resistor	16.5 Ω	—	1%	1206	2	R16, R17
Resistor	10 kΩ	—	5%	1206	1	R59
Resistor	75 Ω	—	5%	1206	4	R18-R20, R57
Resistor	10 Ω	—	5%	0805	1	R56
Resistor	10 kΩ	—	5%	0805	12	R44-R55

Table 4 Recommended Parts List for Physical Layer *(Sheet 2 of 2)*

Description	Value	Volts	Tolerance	Package	Qty	Reference
Resistor	1.5 kΩ	—	5%	0805	7	R11, R41-R62, R43, R60
Resistor	390 Ω	—	5%	0805	4	R12-R15
Resistor	4.7 kΩ	—	5%	0805	8	R34-R40, R64
Resistor	10 Ω	—	1%	0805	2	R31, R32
Resistor	10.5 Ω	—	1%	0805	2	R1, R2
Resistor	40.2 Ω	—	1%	0805	2	R29, R30
Resistor	47.5 Ω	—	1%	0805	2	R4, R5
Resistor	82.5 Ω	—	1%	0805	6	R23-R28
Resistor	130 Ω	—	1%	0805	6	R6-R9, R1, R22
Resistor	511 Ω	—	1%	0805	1	R10
Resistor	TBD	—	1%	0805	2	R33, R65
Transistor	—	—	—	sot23	4	Q1-Q4
DP83223A	—	—	—	28PLCC	1	U2
DP83840	—	—	—	PQFP100	1	U1
Fuse	—	—	—	Radial	1	F1
10/100 Magnetics	—	—	—	SMD	1	T1

Summary

National Semiconductor provides a complete physical solution for 10/100 Ethernet. The component values and design suggestions in this note might vary for a given application. This National Semiconductor application note illustrates the function of the various components and how they relate to system performance. With this information the system designer can modify the recommendations with an understanding of the potential impact.

Note: This is a design recommendation and National Semiconductor is presently investigating this approach in the laboratory and through computer simulation. These results will be made available to National Semiconductor customers.

3 ICS 1890 PHY Network Implementation

The ICS 1890 PHY transceiver integrates all physical layer functions of the IEEE 802.3 10BASE-T and 100BASE-TX from the MII to the isolation transformer of the 10/100-Mb/s magnetics module. This device allows system designers to implement the entire 10/100-Mb/s physical layer channel with one chip, using five passive components to support the onchip analog circuitry, while keeping the total physical layer power consumption under one watt. This section describes how to implement a 10/100-Mb/s adapter using the Digital Semiconductor 21140A and the ICS 1890.

3.1 Overview

The ICS 1890 incorporates an MII allowing easy connection to Digital Semiconductor's media access control (MAC) layer. The interface operates in IEEE standard MII mode for both 10BASE-T and 100BASE-TX.

The ICS 1890 employs autonegotiation logic which has the following three main features:

- Determines the capabilities of the remote link partner.
- Advertises its own capabilities to the remote link partner.
- Automatically adjusts to the highest performance common operating mode.

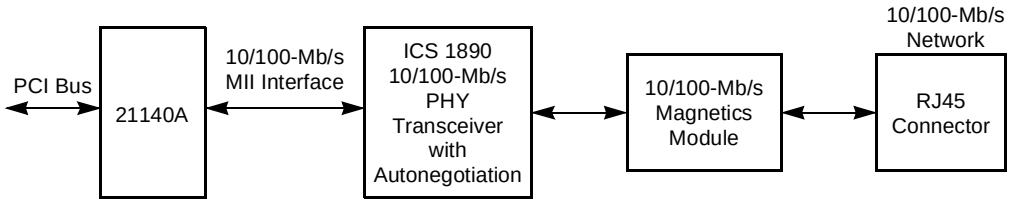
The ICS 1890 autonegotiation logic is designed to operate with legacy 10BASE-T networks or newer systems with multiple connection technology options. When operating with a legacy 10BASE-T remote partner, the ICS 1890 selects the 10BASE-T operating mode transparently to the remote partner. This allows the preservation of existing legacy network structures without management intervention. Legacy 100BASE-TX devices that do not support autonegotiation are also identified and handled by the ICS 1890.

3.2 ICS 1890 Block Diagram

Figure 6 shows the physical layer design for the 10BASE-T and 100BASE-TX ICS 1890 single chip implementation and standard MII interface to the 21140A MAC.

The ICS 1890 implements a fully compliant IEEE 802.3u MII for connection to MACs or repeaters. This allows connection between the ICS 1890 and MAC either on the same board, on a mother/daughter board, or using a cable in a similar manner to the AUI connections.

Figure 6 ICS 1890 System Block Diagram



3.3 ICS 1890 Schematic Diagram Description

Figure 18 shows a schematic diagram of the ICS 1890. This subsection provides a schematic description of the implementation of a complete 10/100-Mb/s physical layer transceiver application from the MII to the RJ45 connector, using the ICS 1890.

The ICS 1890 connects directly to the MII and requires only five additional passive components to set transmit currents and match impedances. In addition, the design is comprised of the following components:

- 25-MHz clock oscillator
- MII PHY address LED or resistor
- Off the shelf, 10/100-Mb/s magnetics module
- Unused pair of termination resistors
- Normal bypass and decoupling capacitors

3.3.1 MII Data Interface

The MII data interface is a specification of signals and protocols that formalizes the interface of a 10/100-Mb/s Ethernet MAC to the underlying physical layer. This specification supports 100BASE-TX, 100BASE-T4, and 100BASE-FX physical type media transparently to the MAC.

The MII data interface specifies both a 4-bit transmit path and a 4-bit receive path allowing for the transfer of a data nibble. The transmit path includes a transmit clock for synchronous transfers, a transmit enable signal, and a transmit error signal. The receive path includes a receive data clock for synchronous transfers, a receive data valid signal, and a receive error signal. The ICS 1890 sources both the transmit clock and receive clock.

The ICS 1890 provides the MII signals carrier sense and collision detect. The following table describes the operation of these signals.

In...	Carrier sense indicates...	Collision detect...
Half-duplex mode	Data is being transmitted or received.	Indicates data has been received while a transmission is in progress.
Full-duplex mode	Data is being received.	Always remains low. Collisions never occur in this mode.

Table 5 maps the 21140A MII interface to the ICS 1890 MII interface.

Table 5 21140A to ICS 1890 MII Interface Signal Mapping *(Sheet 1 of 2)*

Signal	21140A	Pin	ICS 1890	Pin
Transmit clock	**mii/sym_tclk**	123	TXCLK	43
Transmit enable	**mii/sym_txen**	125	TXEN	44
Transmit error	**—**	—	TXER[1]	42
Transmit data 3	**mii/sym_txd<3>**	131	TXD3	48
Transmit data 2	**mii/sym_txd<2>**	130	TXD2	47
Transmit data 1	**mii/sym_txd<1>**	127	TXD1	46
Transmit data 0	**mii/sym_txd<0>**	126	TXD0	45

Table 5 21140A to ICS 1890 MII Interface Signal Mapping *(Sheet 2 of 2)*

Signal	21140A	Pin	ICS 1890	Pin
Receive clock	**mii/sym_rclk**	114	RXCLK	37
Data valid	**mii_dv**	111	RXDV	36
Receive error	**mii_err**	110	RXER	38
Receive data 3	**mii/sym_rxd<3>**	118	RXD3	32
Receive data 2	**mii/sym_rxd<2>**	117	RXD2	33
Receive data 1	**mii/sym_rxd<1>**	116	RXD1	34
Receive data 0	**mii/sym_rxd<0>**	115	RXD0	35
Carrier sense	**mii_crs**	113	CRS	50
Carrier detect	**mii_clsn**	112	COL	49
Management data clock	**mii_mdc**	106	MDC	31
Management data input/output	**mii_mdio**	105	MDIO	30

[1] The 21140A does not support the transmit error function, so this pin should be grounded.

3.3.2 LED and PHY Pins

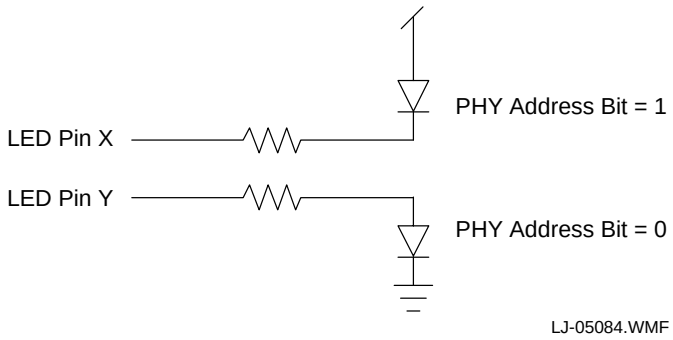
The ICS 1890 device uses a unique pin sharing scheme that allows the five LED pins to also be used to set the PHY address. During power up and reset, these pins set the PHY address of the device. Following power up and reset, these pins are used as LED status indicators.

The PHY address can be any number from 0 to 31. If a PHY address of 0 is used, the MII interface is isolated on power up or reset and must be explicitly enabled through the MII management port (register 0, bit 10) as defined by the IEEE specification. All other address selections leave the MII interface active by default.

If both the 21140A and the ICS 1890 are mounted directly on the same printed circuit board, a PHY address of 1 is a good choice.

The PHY address is set by the configuration of the LED components (Figure 7). When a value of 1 is needed, the LED and resistor are connected between the LED pin and **Vdd** (LED pin X example). When a value of 0 is needed, the LED and resistor are connected between the LED pin and ground (LED pin Y example). The special driver in the ICS 1890 senses the polarity and adjusts its drive logic to appropriately turn the LED on or off. Resistor values should be in the range of 510 Ω to 10 kΩ (1/2 W). The recommended resistor value is 1 kΩ (1/2 W).

Figure 7 LED Status and PHY Addressing



If LEDs are not required for your application, only a resistor is required to set the PHY address.

3.3.3 ICS 1890 Power Supply Isolation, Filtering, and Layout Considerations

It is very important to properly isolate the ICS 1890 10/100-Mb/s Physical Layer Device from noise sources in a system design. Two main areas of consideration include:

- Isolation from 21140A noise.
- Noise coupling between the ICS 1890 transmitter and receiver.

Two methods can be used to isolate the 21140A, transmit, and receive power supplies.

Method	Description
Using a single **Vdd** plane	Isolate the supply domains with ferrite beads and point-to-point routing as described in Table 6 and Figure 8. The corresponding ground pins are tied directly below to a single internal layer ground plane.
Using split **Vdd** planes	Connect the power pins to the planes directly below them (except for pin 56 which must be point-to-point trace routed as shown in Figure 9). As with the single **Vdd** method, all ground pins are tied directly below to a single ground plane.

For both methods, ICS 1890 filtering is accomplished by separating the power supply into three domains: 21140A, transmit, and receive. Table 6 lists all supply pins on the device into one of these three categories. Each supply pin is followed directly by its corresponding ground pin. Supply pins are shown paired up with their appropriate neighbor for bypass purposes. All ground pins are tied to a single ground plane below. Each supply pair should be bypassed with a 0.1-µF capacitor located as close to the device as possible.

Table 6 Power Supply Filtering

21140A Domain	Transmit Domain	Receive Domain
41 **Vdd** 40 **Vss**	8 **Vdd** 7 **Vss**	16 **Vdd** 18 **Vdd** 17 **Vss**
54 **Vdd** 51 **Vss**	56 **Vdd** 55 **Vss**	25 **Vdd** 29 **Vss**
57 **Vdd** 63 **Vss**		

Figure 8 illustrates a single **Vdd** plane isolation with point-to-point trace routing. The 21140A domain **Vdd** pins drop directly down to the single power plane while the transmit and receive domain pins are isolated using point-to-point routing and inline ferrite beads.

Figure 8 Single Vdd Plane Isolation

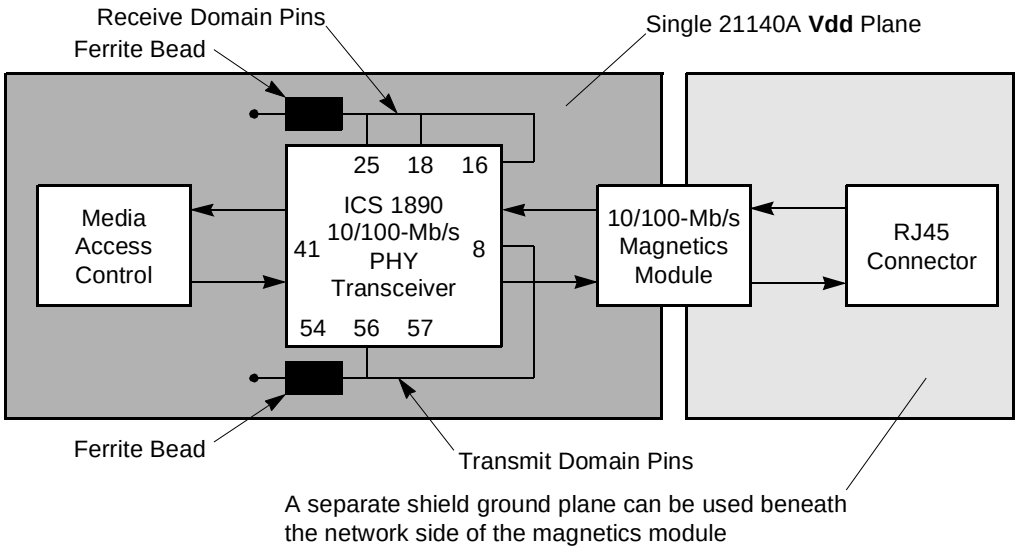
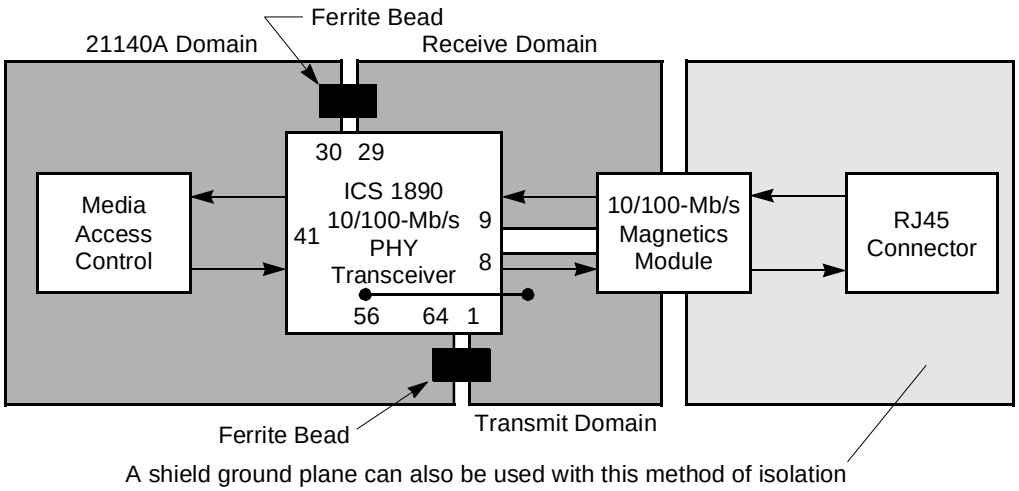


Figure 9 illustrates split **Vdd** planes power supply isolation. The power planes must be split as shown in this figure. The pin number callouts specify where the power plane splits should occur in the board. Note that pin 56, transmit **Vdd**, is above the 21140A domain **Vdd** plane. This pin must be point-to-point trace routed to the transmit domain power plane as shown. All other power pins besides pin 56 connect directly to their corresponding power planes below them. A single, uniform plane should be used for ground. Both the receive and transmit domains should be connected to the 21140A domain through a ferrite bead or inductor.

Figure 9 Split Vdd Plane Isolation



3.3.4 ICS 1890 Power Management Considerations

The ICS 1890 supports the following two power-saving modes:

- Low power mode is used to reduce power consumption in the device. Low power mode is activated by holding the RESET pin continuously low or by writing a logic 1 to the power-down bit (status register 0, bit 11). When the device is in low power mode, all functions are disabled except for register accesses through the MII management interface. All register values are maintained during low power mode, except for latching status bits which are reset to their default values.
- Automatic 100BASE-T power-down is used to reduce its total power requirements when operating in 10BASE-T mode by automatically powering down the 100BASE-TX modules. The power consumption value for each mode is listed in Table 7.

Table 7 Power Consumption Values *(Sheet 1 of 2)*

Power Parameters	Power Modes	Power Values
Total power consumption	—	Less than one watt maximum. Supply current 195 mA maximum.
Low power	System reset	Pin 22 held low causes ICS 1890 to reset and enter low power mode. Supply current approximately 30 mA.

Table 7 Power Consumption Values *(Sheet 2 of 2)*

Power Parameters	Power Modes	Power Values
	Power-down	Status register 0, bit 11, set to a logic 1 causes the ICS 1890 to enter low power mode with only management interface and logic remaining active. This action isolates the transmit data output and the MII. Supply current approximately 30 mA.
	Reference input stop	When the 25-MHz clock signal is removed (or stopped), the ICS 1890 supply current drops to approximately 30 mA.
	Automatic 100BASE-TX power-down	Extended control register 2 (register 19), setting bit 0 to a logic 1 with 10BASE-T selected for network connection, automatically turns off the 100BASE-TX transceiver. Automatic 100BASE-TX power-down mode supply current is approximately 100 mA.

Note: Power-down mode supply current values are not tested and are approximated. ICS advises its customers to obtain the latest version of all device data from ICS to verify that any information being relied on by the customer is current and accurate.

4 Broadcom BCM5000 Chip Implementation

This section describes how to interface the Digital Semiconductor 21140A with the Broadcom BCM5000 10/100BASE-T4 Fast-Φ™ (referred to as the BCM5000).

4.1 Overview

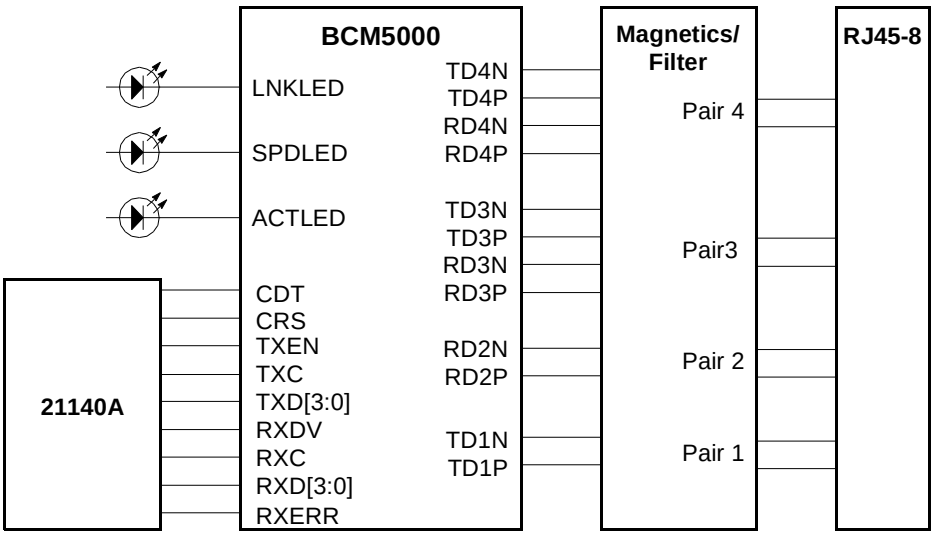
The BCM5000 is a single CMOS chip that performs all the physical layer interface functions for 100BASE-T4, 10BASE-T, and 10BASE-T full-duplex Ethernet on CAT3, 4, or 5 unshielded twisted-pair (UTP) cable. The BCM5000 is fully compliant with the IEEE 802.3 and IEEE 802.3u specifications. The BCM5000 is also fully compliant with the media-independent interface (MII) specification.

The chip receives and transmits data on UTP in the form of 8B6T for 100BASE-T4, and Manchester code for 10BASE-T. The BCM5000 connects directly to the T4 magnetics and recovers data and clock from the incoming signals. The recovered data stream is then decoded and output through the MII interface. For packet transmission, the binary data stream is received through the MII interface, encoded and then transmitted through the interpolating line drivers out to the T4 magnetics.

4.2 Block Diagram

Figure 10 is a block diagram of an adapter based on the 21140A and the BCM5000.

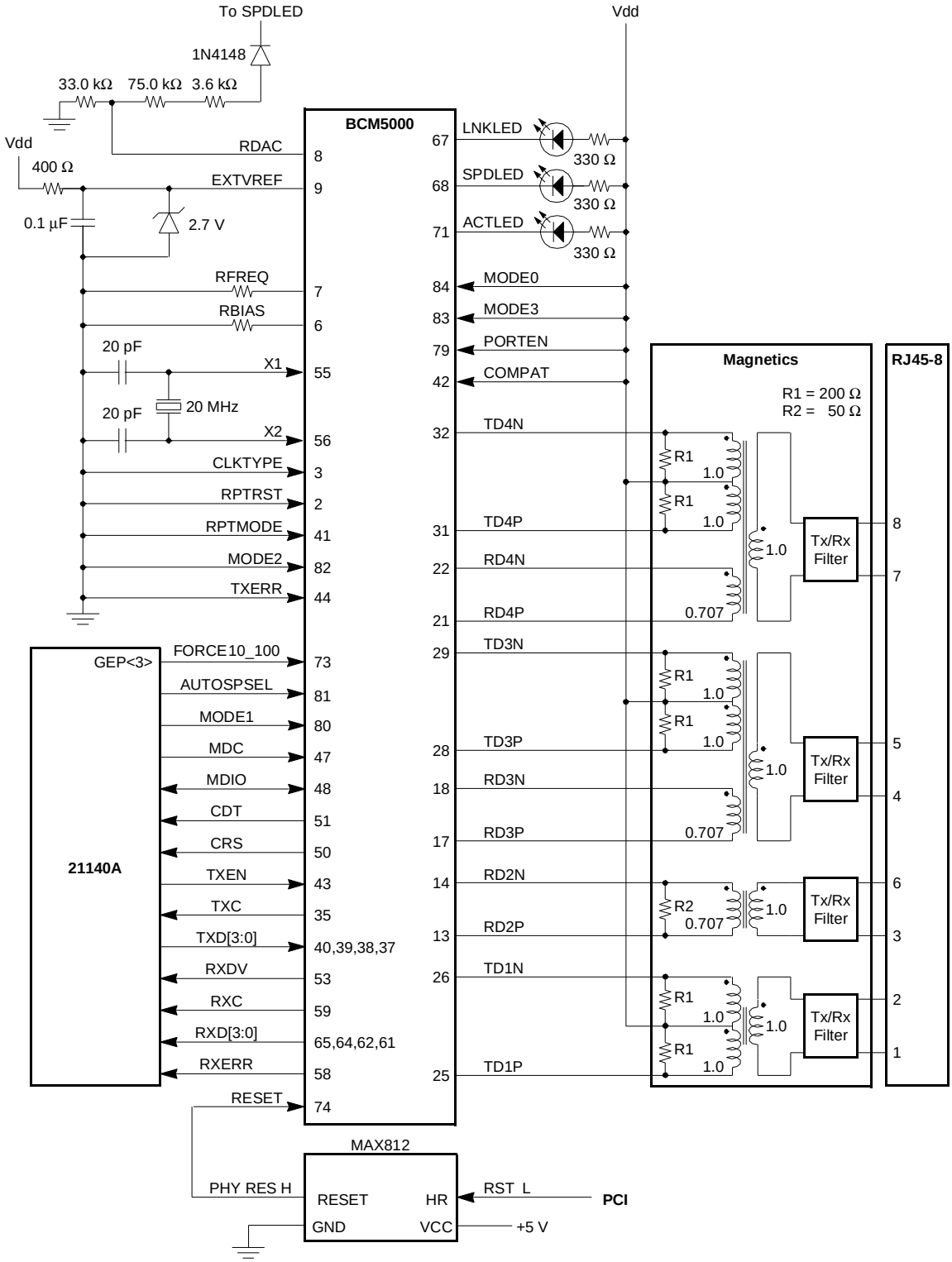
Figure 10 Adapter Card Application



4.3 Schematics

Figure 11 shows how to connect the BCM5000 to the 21140A.

Figure 11 BCM5000 in MII Mode with 20-MHz Crystal



The BCM5000 requires a hardware reset on power-up. Subsequent resets, if required, might be done in software through the MII management interface. The following are some possible ways to generate the hardware reset:

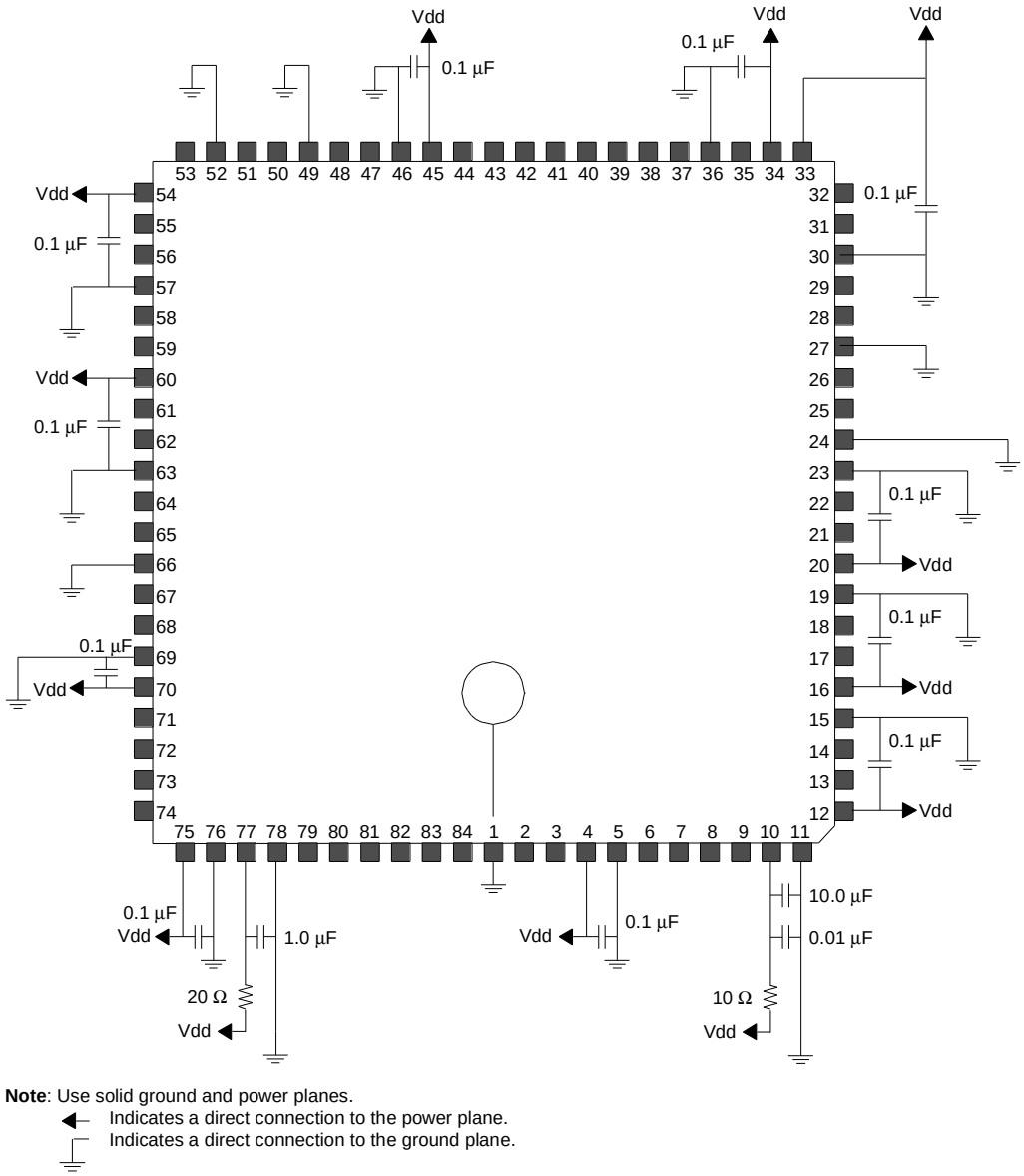
- Use the PCI reset. Because the PCI specification requires that PCI signals drive only one load, the reset should be buffered as it comes off the connector. The buffered signal can then be used to reset the 21140A and the BCM5000.
- Use an RC circuit to generate a reset pulse following power-up.
- Use a reset generator chip.
- Connect one of the general-purpose pins in the 21140A to the BCM5000 reset and apply a reset pulse to the BCM5000 through the driver.

A 20-MHz or 50-MHz oscillator can be used rather than a 20-MHz crystal. When using an oscillator, the 20-pF capacitors are not required. The oscillator should be 100 ppm.

4.4 Power Requirements

Figure 12 shows the recommended power supply connections using the BCM5000. Solid power and ground planes should be used.

Figure 12 Recommended Power Supply Connections



Note: Use solid ground and power planes.

Indicates a direct connection to the power plane.

Indicates a direct connection to the ground plane.

Table 8 lists the components required for this application.

Table 8 BCM5000 Application Parts List

Description	Qty	Value	Tolerance	Vendor	Part Number	Comments
10/100BASE-T4 PHY	1	—	—	Broadcom	BCM5000	—
Magnetics	1	—	—	Valor Pulse Engineering Fil-Mag	SF6036 PE69025 78Z-9022SM	—
RJ45-8 connector	1	—	—	—	—	—
Crystal	1	20 MHz	—	—	—	50 ppm crystal tuned to equivalent load of 15 pF[1]
Zener diode	1	2.7 V	±5%	—	—	—
LED	3	—	—	—	—	—
Diode	1	—	—	—	1N4148	—
Resistor	3	27 kΩ	±1%	—	—	RFREQ, RBIAS
Resistor	1	33 kΩ	±1%	—	—	RDAC
Resistor	1	75 kΩ	±1%	—	—	RDAC
Resistor	1	3.6 kΩ	±1%	—	—	RDAC
Resistor	1	400 Ω	±1%	—	—	—
Resistor	1	330 Ω	±1%	—	—	—
Resistor	1	20 Ω	±5%	—	—	—
Resistor	1	10 Ω	±5%	—	—	—
Capacitor	11	0.1 µF	—	—	—	—
Capacitor	1	1 µF	—	—	—	—
Capacitor	1	10 µF	—	—	—	—
Capacitor	2	20 pF	—	—	—	—

[1] A 20-MHz or 50-MHz oscillator can be used rather than a 20-MHz crystal. When using an oscillator, the 20-pF capacitors are not required. The oscillator should be 100 ppm.

4.5 Layout Considerations

- Single power and ground planes should be used.
- The power and ground planes should be cut out from under the RJ45-8 and the portion of the magnetics component that interfaces to the RJ45-8.
- The high frequency lines should be kept as short as possible.
- The crystal oscillator should be placed as close to the BCM5000 as possible.
- Clocks and other high frequency lines should not cross over the transmit and receive lines connecting the BCM5000 to the magnetics.
- Bypass capacitors should be placed between the power and ground planes.
- When using multiple BCM5000 chips in a single application, care should be taken in routing signals to the magnetics parts to avoid cross talk between the signals.

A National Semiconductor Common Magnetics License Agreement and Design Recommendations

A.1 Common Magnetics License Agreement

Dear Customer:

The attached or enclosed application note describes the use of the National Semiconductor Corporation's recommended 10/100 Physical layer front end using the National Semiconductor Corporation's part number DP83840VCE 10/100 Mb/s Ethernet Physical Layer and National Semiconductor Corporation's Part Number DP83223.

The following suppliers have indicated that they are or will provide magnetic parts for the National Semiconductor Corporation recommended implementation. National Semiconductor makes no warranty as to the suitability of any of the Common Magnetics Suppliers listed unless they are listed on a "National Semiconductor Approved Supplier list".

The attached application note describes the recommended application of the following magnetic part(s):

Bel Fuse	0558-3899-00
Fil-Mag Technical	78Z479
Halo Electronics	TD22-3506G1
Kappa Technology	FM2211GW
Nano Pulse	NPI6170-30
PCA	EPF8001
Pulse Engineering	PE68515
Valor Electronics	PT4171

Which is in conjunction with National Semiconductor Corporation's part number DP83840VCE 10/100 Mb/s Ethernet Physical Layer and National Semiconductor Corporation's part number DP83223 components. The above referenced magnetics part(s) have designed as a common magnetics front end for use with both of these NSC components. This system provides combination 10BASE-T and 100BASE-T capabilities.

The system and methods of operation thereof are covered by one or more pending patents of National Semiconductor Corporation. Purchasers of both National Semiconductor Corporation's DP83840VCE 10/100 Mb/s Ethernet Physical layer and DP83223 components are hereby granted by National semiconductor Corporation a non-exclusive, paid-up, non-transferable license under such pending patents and those patents which issue therefrom, to make, use and sell such systems **which utilize both of National Semiconductor Corporation's DP83840VCE 10/100 Mb/s Ethernet Physical layer and DP83223 components.** National Semiconductor Corporation's part number DP83223 is covered by U.S. Patent Nos. 5,337,025 and 5,444,410.

A.2 National Semiconductor Physical Layer Design Recommendations

The following schematics represent the National Semiconductor 10/100 Ethernet Physical Layer design recommendations. This implementation might vary from the Digital Semiconductor Reference Design, due to the designer's preferences, and might differ from any other given application implementation as well. Again these recommendations are intended to improve the designer's understanding of Fast Ethernet systems, and with that understanding a designer is able to develop systems more effectively.

Note: The value of C8 should be 820 pF instead of 1000 pF as shown in Figure 16.

Figure 13 10/100 Ethernet Physical Layer Block Diagram

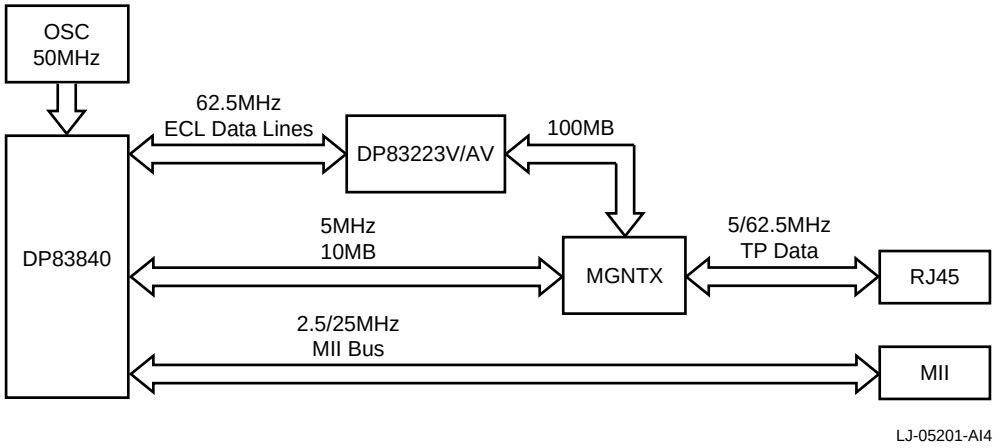


Figure 14 DP83840

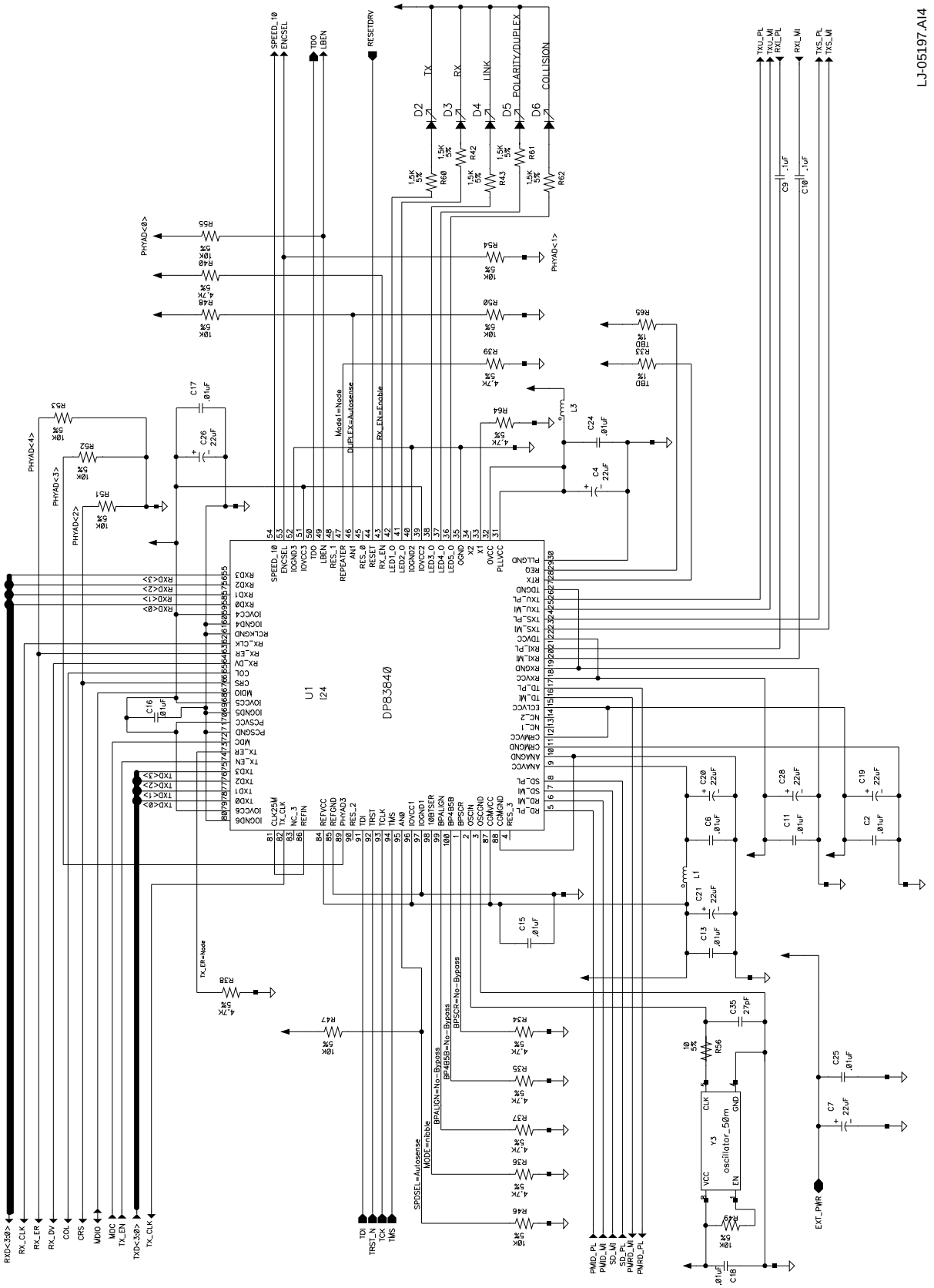


Figure 15 DP83223

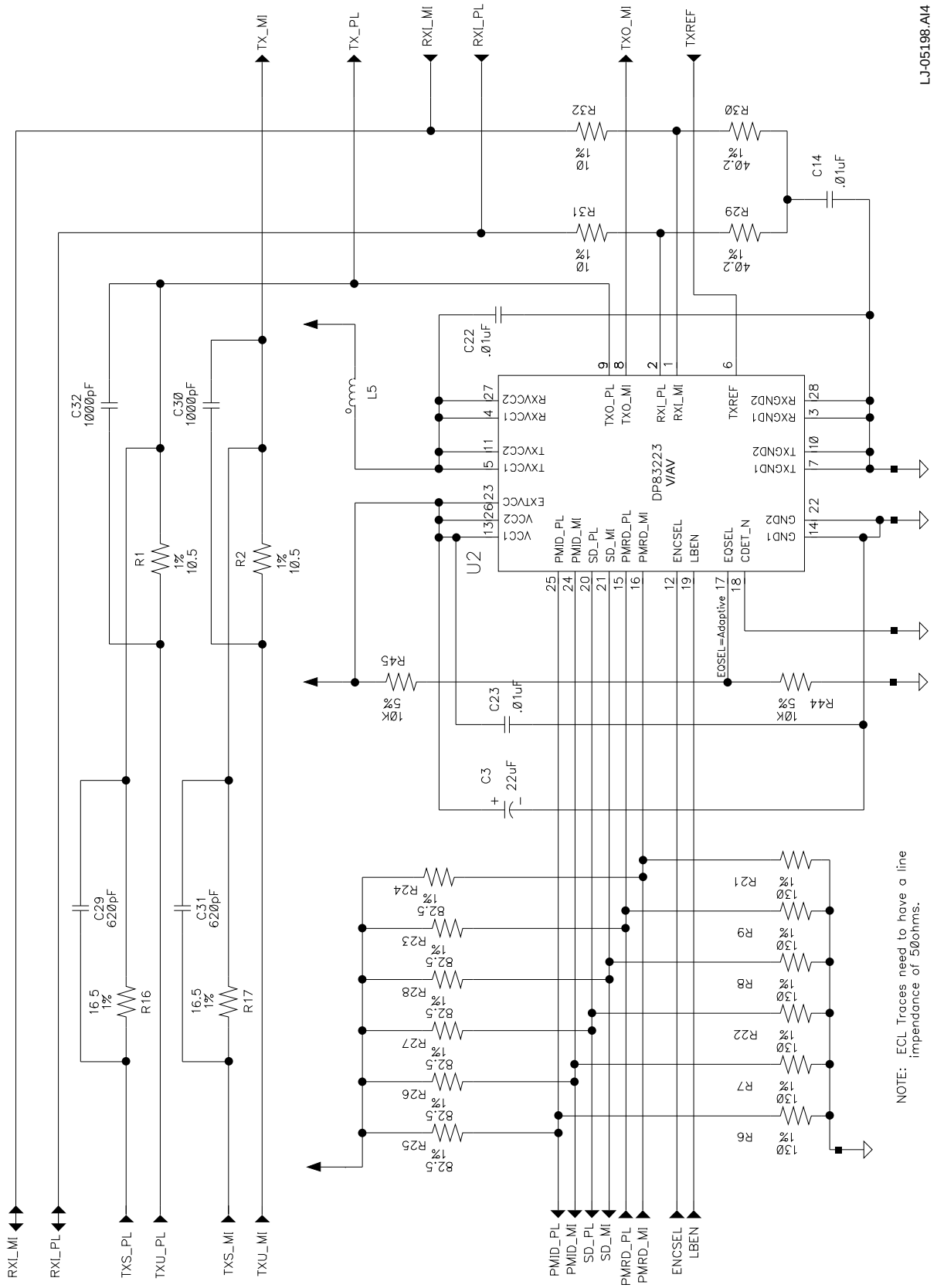


Figure 16 Twisted-Pair

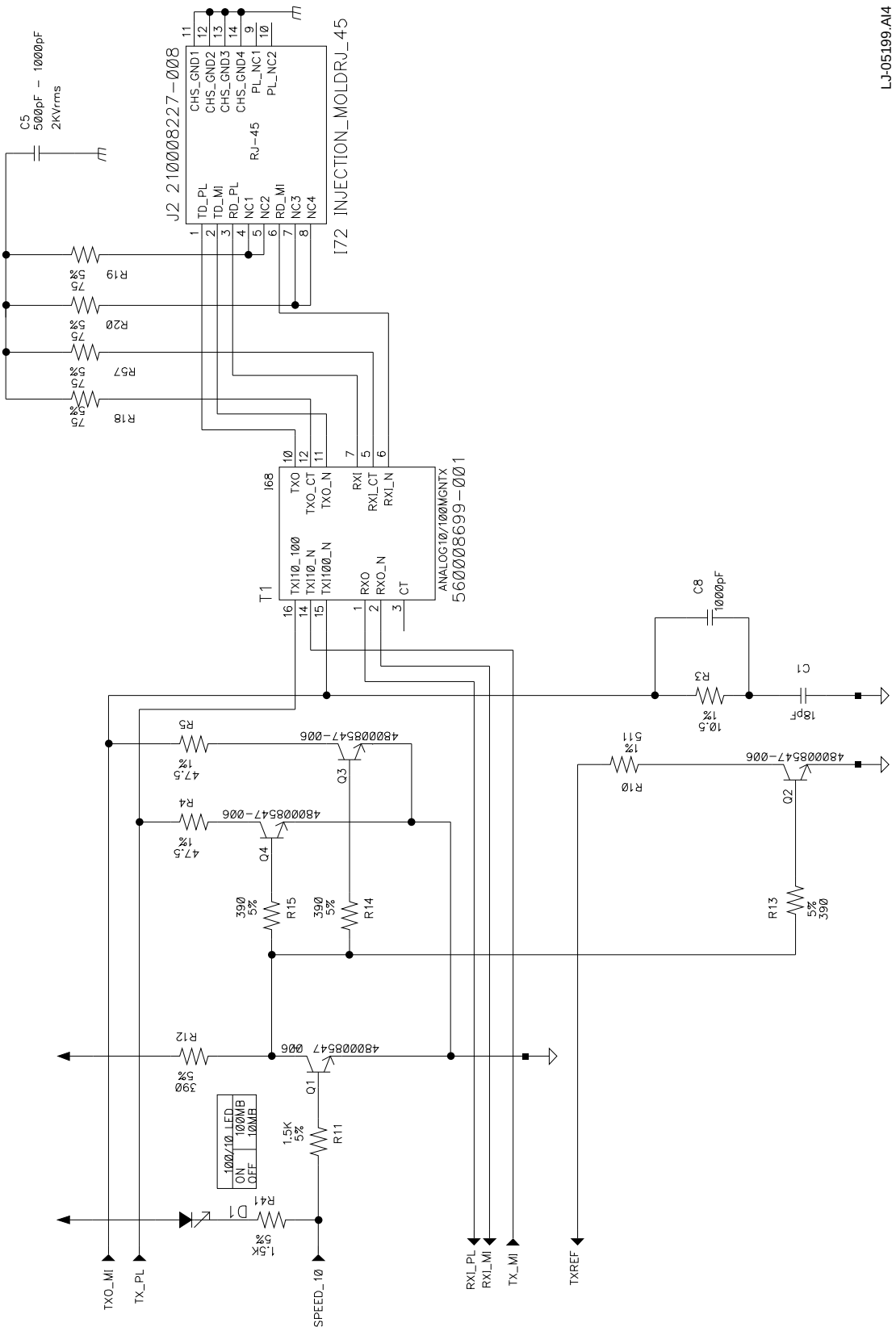
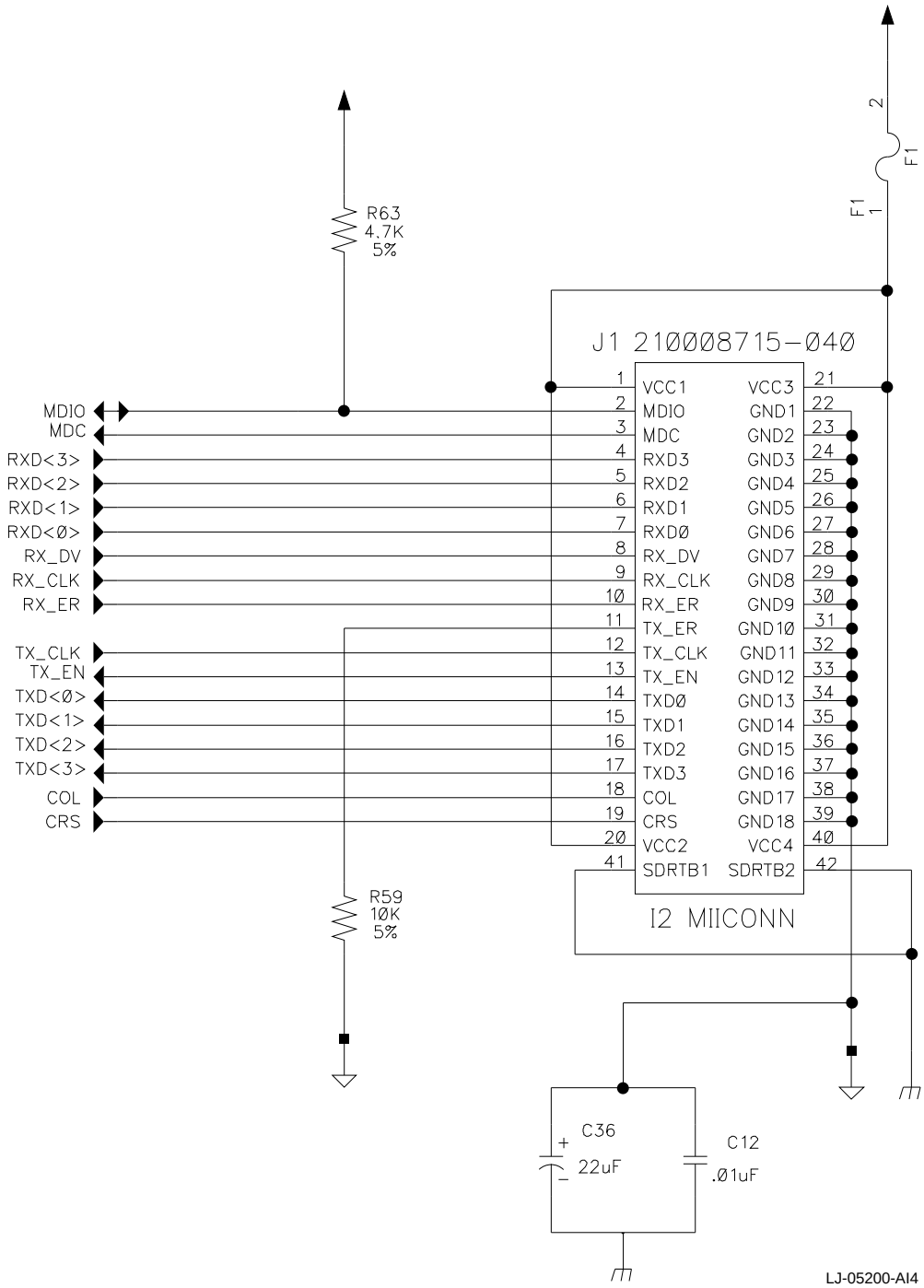


Figure 17 MII Interface



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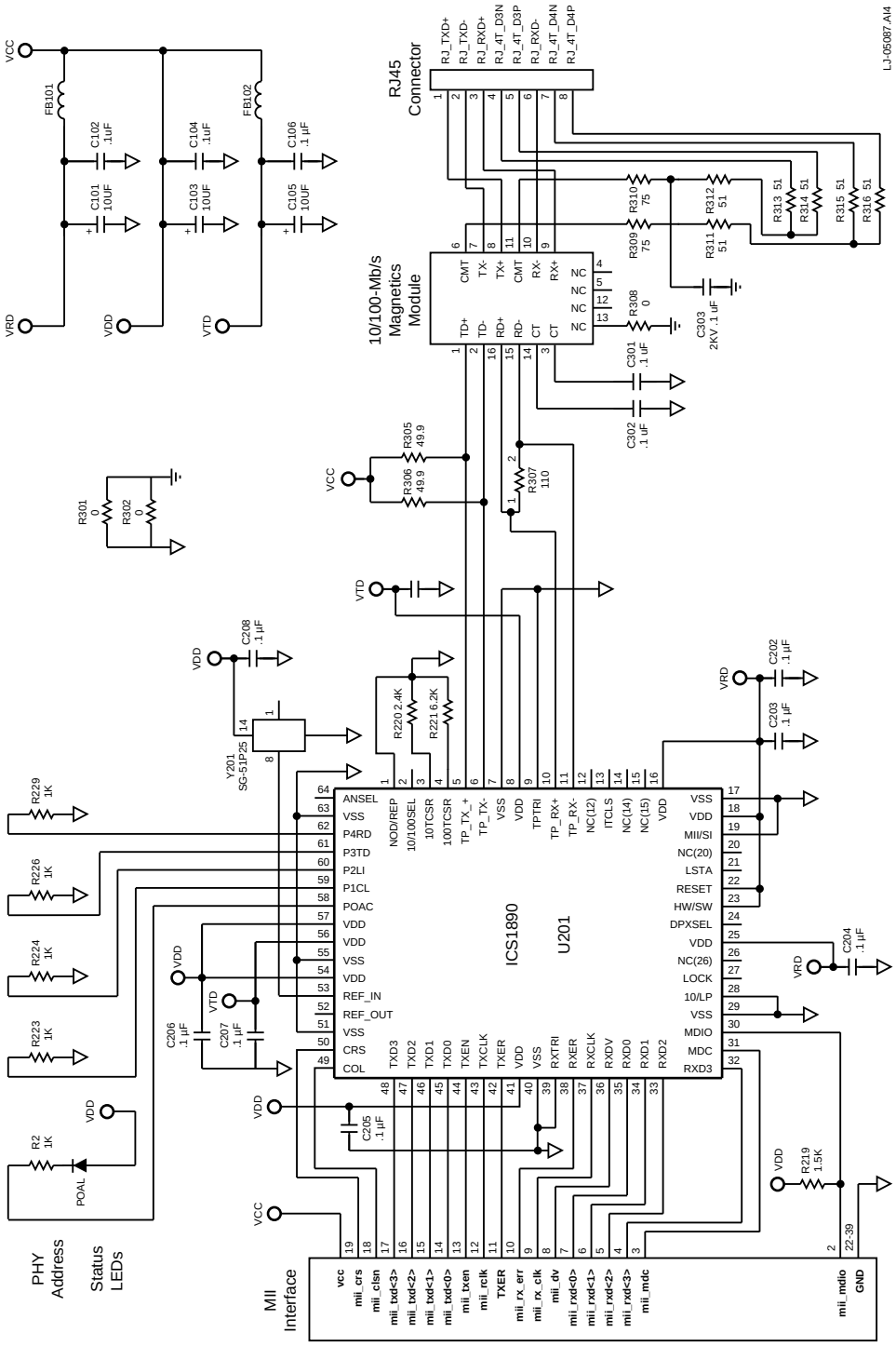
B ICS 1890 PHY Schematic Information

This appendix provides detailed schematic type information for the ICS 1890 PHY. It also provides an ICS 1890 PHY external component listing and information for selecting a 10/100-Mb/s magnetics module that is compatible with the ICS 1890 PHY.

B.1 ICS 1890 Schematic Diagram

Figure 18 is a schematic diagram of the ICS 1890.

Figure 18 ICS 1890 Schematic Diagram



B.2 ICS 1890 External Component Listing

Table 9 lists the external components used with the ICS 1890 in Figure 18. Only five resistors are required for the analog circuitry build. Two of the resistors are used to set, precisely, transmit currents for 10BASE-T and 100BASE-TX. The remaining three resistors are used to match the impedance of the twisted-pair cabling. Other components are used optionally to enhance system design when using an MII connector or multiple LED indicators.

Table 9 ICS 1890 External Components

Component	Description	Qty	Comments
Resistor	2.4 kΩ, 1/2 W, 1%	1	10BASE-T transmit current setting.
Resistor	6.2 kΩ, 1/2 W, 1%	1	100BASE-TX transmit current setting.
Resistors	49.9 Ω, 1/2 W, 1%	2	Impedance matching.
Resistor	110 Ω, 1/2 W, 1%	1	Impedance matching.
Resistors[1]	51 Ω, 1/2 W	6	Unused twisted-pair terminations, for termination if desired.
Resistors[1]	75 Ω, 1/2 W	2	Unused twisted-pair terminations, for termination if desired.
Resistor[1]	1.5 kΩ, 1/2 W	1	MDIO pull-up, optional if internal to the MAC.
Resistors[1]	1 kΩ, 1/2 W	5	For LEDs (nominal range 510 Ω to 10 kΩ, 1/2 W).
Capacitors	0.1 µF	14	For supply bypass.
Capacitors	10 µF	3	For supply decoupling.
LED[1]	—	1	—
Ferrite Beads or Inductors	—	2	21140A and transmit/receive isolation.
10/100-Mb/s Magnetics Module	—	1	Appendix B.3 provides recommendations.
Oscillator[1]	25 MHz, ±50 PPM	1	Values true for all conditions. A frequency reference with the same performance can also be substituted.
RJ45 Connector	—	1	Network connection.

[1] Component(s) not required for all system designs.

B.3 10/100-Mb/s Magnetics Module Selection

Table 10 lists some of the vendor magnetic modules that are compatible with the ICS 1890 10/100-Mb/s, twisted- pair, PHY transceiver. These modules are off the shelf type modules designed for use with 10/100-Mb/s Ethernet devices.

Two configuration styles are available:

- No choke style
- Extra choke style

The no choke style in Figure 19 has an exposed center tap on the transmit side, therefore, it does not have a primary side common-mode choke.

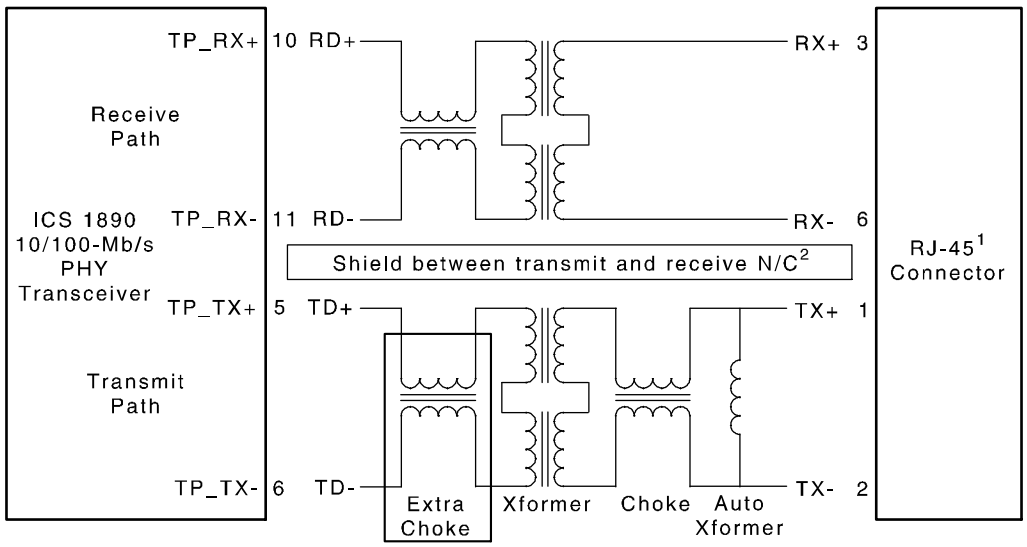
The extra choke style adds a common-mode choke to the primary of the transmit side. This is possible because the ICS 1890 drives the transmitter 1:1 for both 10BASE-T and 100BASE-TX.

Table 10 lists the two configuration styles of transformers. A number of pin compatible modules from different vendors are listed. Figure 20 shows the footprints for both the no choke style and extra choke style transformers.

Table 10 10/100-Mb/s Magnetic Module Vendors

Manufacturer	No Choke Style Part Number	Extra Choke Style Part Number
Bel Fuse	—	S558-5999-01
Halo (singles)		
Extra choke	TG32-3506ND	TG22-S010ND
No choke	TG22-3506ND	—
3-wire choke (in place of autotransfomer)	TG32-S020ND	—
Nano Pulse	NP16170-30	NP16120-30
Pulse Engineering	PE-68515	PE-68517
Valor	ST6118	ST6114
Nano Pulse (SIP package)	—	NP16120-00

Figure 19 10/100-Mb/s Magnetics Module Data Paths

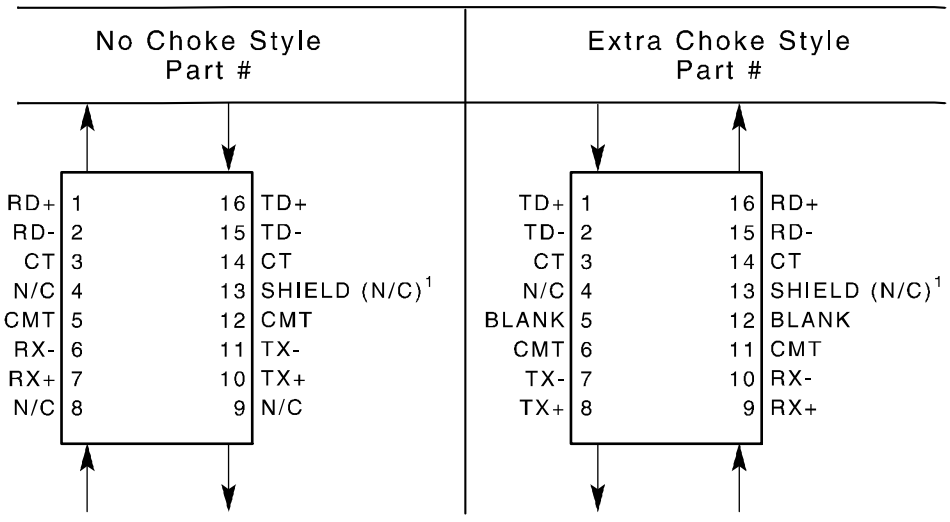


[1] The RJ-45 pinout shown is for the NIC side of the link. The hub side typically implements crossover function by swapping the 3 and 6 and 1 and 2 pairs.

[2] The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

LJ-05124.WMF

Figure 20 No Choke, Extra Choke Style Transformer Footprints



[1] The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

LJ-05125.AI4

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To obtain a *Digital Semiconductor Product Catalog,* call the Digital Semiconductor Information Line. The following table lists some of the semiconductor products available from Digital Semiconductor:

Product	Order Number
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller	21140-AC
Digital Semiconductor 21140A Evaluation Board Kit	21A40-TX
Digital Semiconductor 21142 10/100-Mb/s Ethernet LAN Controller (PQFP package)	21142-PA
Digital Semiconductor 21142 10/100-Mb/s Ethernet LAN Controller (TQFP package)	21142TA

Ordering Associated Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, call the Digital Semiconductor Information Line.

Title	Order Number
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Product Brief	EC–QN7MB–TE
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Data Sheet	EC–QN7PD–TE
Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual	EC-QN7ND-TE
Digital Semiconductor 21142 10/100-Mb/s Ethernet LAN Controller Product Brief	EC–QPNTB–TE
Digital Semiconductor 21142 10/100-Mb/s Ethernet LAN Controller Data Sheet	EC–QPNUB–TE
Digital Semiconductor 21142 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual	EC-QPNVA-TE

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Ordering Broadcom Products

The following table lists Broadcom available 100BASE-T4 PHY related products.

Product	Order Number
BCM5000 10/100BASE-T4 Fast-Φ chip (84-pin PLCC package)	BCM5000 KPJ
BCM5000 10/100BASE-T4 Fast-Φ chip (100-pin PQFP)	BCM5000 KPF

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You can order the following literature directly from Broadcom Corporation:

Title	Vendor
BCM5000 10/100BASE-T4 Fast-Φ Transceiver data sheet Application note for BCM5000 10/100BASE-T4 Fast-Φ Transceiver Schematic set for the BCM5000 PCI 100BASE-T4 Adapter based on the 21140A	Broadcom Corporation, 1–714–450–8700

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Product	Order Number
DP83223A Transceiver product samples	—
DP83840 Physical Layer product samples	—

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Title	Vendor
10/100 Ethernet Common Magnetics application note 10/100 BASE-T Magnetics Specification 1996 National Ethernet Databook DP83223A Transceiver data sheets DP83223 TWISTER Adaptive Equalization Considerations application note DP83840 Physical Layer data sheets System Considerations application note TP-PMD specification Transmission Line Concepts application note Unmanaged Repeater application note	Contact your local National Semiconductor sales representative, or call the National Semiconductor Customer Support center at 1–800–272–9959

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IEEE standards 802.3, 802.3u, and 1149.1	The Institute of Electrical and Electronics Engineers, Inc. U.S. International FAX	 1–800–701–4333 1–908–981–0060 1–908–981–9667