SHARP

Integrated Circuits Group

APPLICATIONS:
- PDA
- Digital Camera

LH28F320S3 32M (4M × 8/2M × 16) Smart 3 Flash Memory

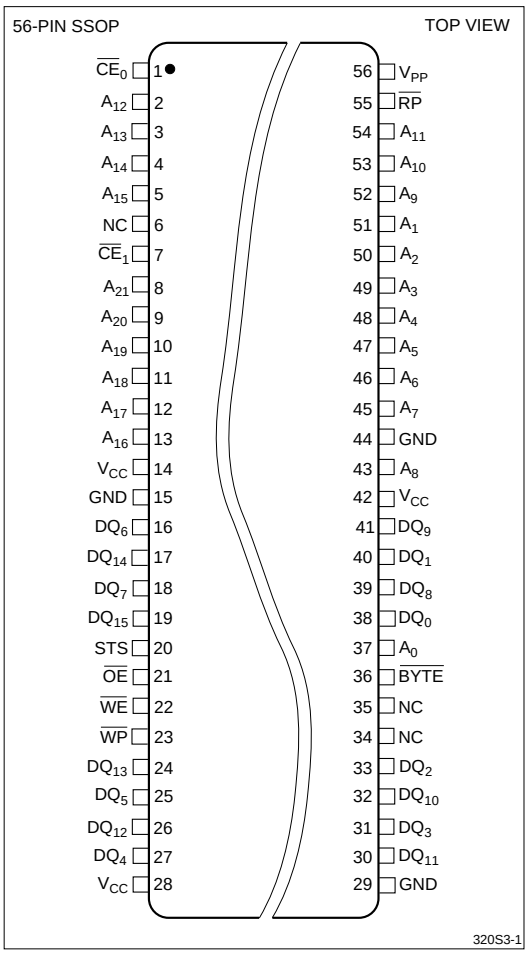
FEATURES

- Smart 3 technology
  - 2.7 V or 3.3 V V_{CC}
  - 2.7 V, 3.3 V or 5 V V_{PP}
- Common flash interface (CFI)
  - Universal and upgradable interface
- Scalable command set (SCS)
- High speed write performance
  - 32 Bytes × 2 plane page buffer
  - 2.7 µs byte write transfer rate
- High speed read performance
  - 110/140 ns (3.3 V ±0.3 V)
  - 130/160 ns (2.7 V – 3.6 V)
- Enhanced automated suspend options
  - Write suspend to read
  - Block erase suspend to write
  - Block erase suspend to read
- Industry-standard packaging
  - 56-pin SSOP
- Chip size packaging
  - 64-ball CSP
- SRAM-compatible write interface
- User-configurable × 8 or × 16 operation
- High-density symmetrically-blocked architecture
  - Sixty-four 64K erasable blocks
- Enhanced data protection features
  - Absolute protection with V_{PP} = GND
  - Flexible block locking
  - Erase/write lockout during power transitions
- Extended cycling capability
  - 100,000 block erase cycles
  - 6.4 million block erase cycles/chip
- Low Power management
  - Deep power-down mode
  - Automatic power savings mode
  - Decreases I_{CC} in static mode
- Automated write and erase
  - Command user interface
  - Status register
- ETOX™ V nonvolatile flash technology
- Not designed or rated as radiation hardened

DESCRIPTION

SHARP's LH28F320S3 Flash memory with Smart 3 technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code and data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320S3 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

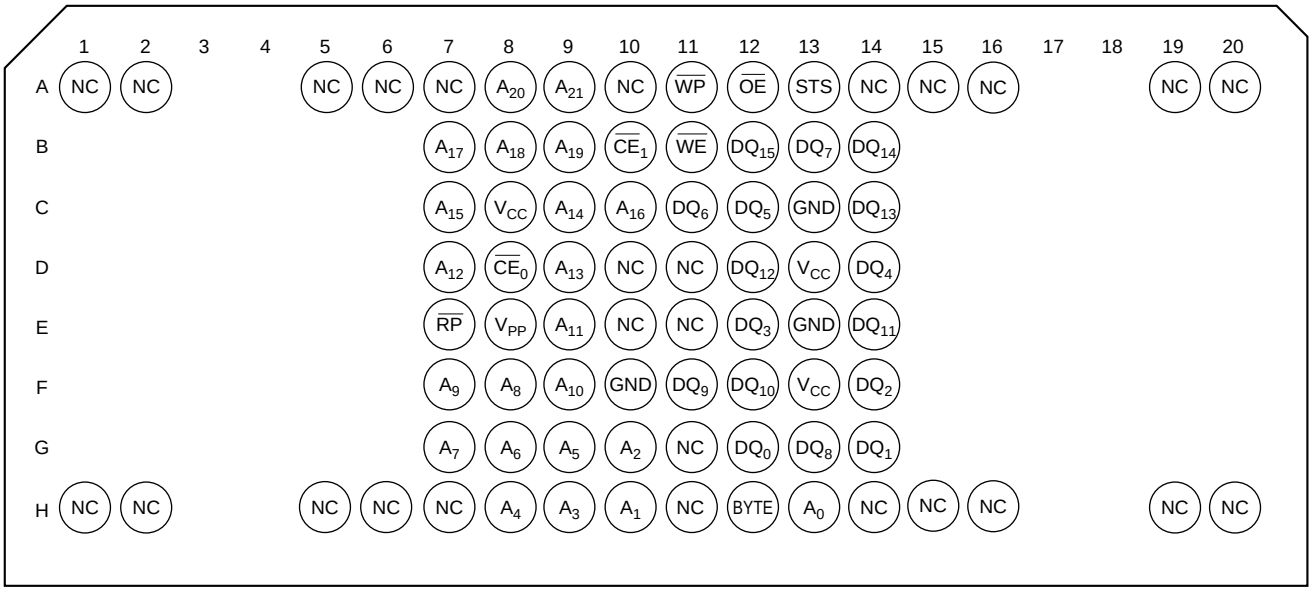
56-PIN SSOP PINOUT



This Product Information is from LH28F320S3 Preliminary Product Preview, Rev. 1.1

64-BALL CSP PINOUT

64-BALL CSP — TOP VIEW



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