# *256K x 16Bit CMOS Dynamic RAM with Extended Data Out*

## DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), Access time (-5,-6 or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 256Kx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

## FEATURES

- **Part Identification**

  - KM416C254D/DL (5V, 512K Ref.)
  - KM416V254D/DL (3.3V, 512K Ref.)

- **Active Power Dissipation**

Unit : mW

| Speed | 3.3V(512 Ref.) | 5V(512 Ref.) |
|---|---|---|
| -5 | - | 605 |
| -6 | 255 | 495 |
| -7 | 235 | 440 |

- **Refresh Cycles**

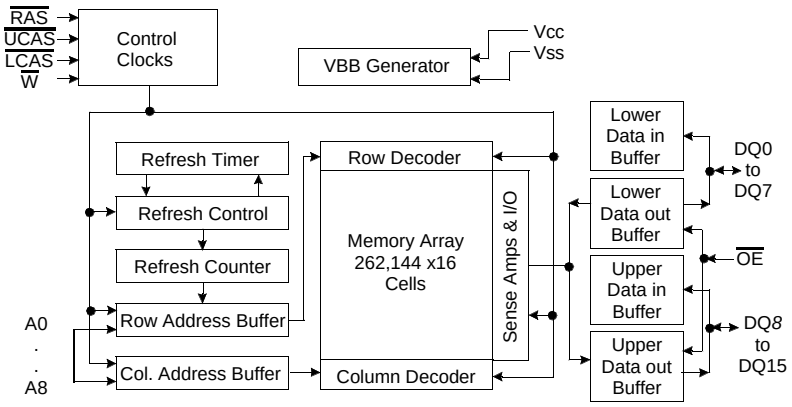
| Part NO. | Vcc | Refresh cycle | Refresh period | |
|---|---|---|---|---|
| | | | Normal | L-ver |
| C254D | 5V | 512K | 8ms | 128ms |
| V254D | 3.3V | | | |

- **Performance Range:**

| Speed | tRAC | tCAC | tRC | tHPC | Remark |
|---|---|---|---|---|---|
| -5 | 50ns | 15ns | 84ns | 20ns | 5V only |
| -6 | 60ns | 15ns | 104ns | 25ns | 5V/3.3V |
| -7 | 70ns | 20ns | 124ns | 30ns | 5V/3.3V |

- Extended Data Out Mode operation
- 2 $\overline{CAS}$ Byte/Wrod Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 40-pin SOJ 400mil and 44(40)-pin TSOP(II) 400mil packages
- Triple +5V¡¾10% power supply (5V product)
- Triple +3.3V¡¾0.3V power supply (3.3V product)

## FUNCTIONAL BLOCK DIAGRAM

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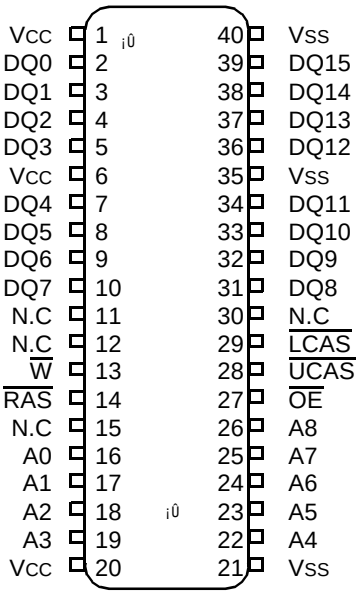
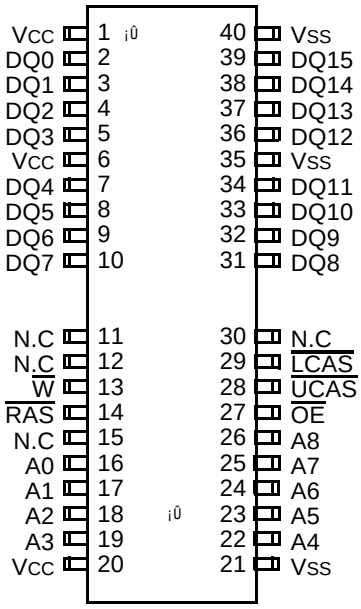
## PIN CONFIGURATION (Top Views)

**KM416C/V254DJ**




**(SOJ)**

**KM416C/V254DT**




**(TSOP-II)**

| Pin Name | Pin Function |
|---|---|
| A0 - A8 | Address Inputs |
| DQ0 - 15 | Data In/Out |
| VSS | Ground |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{UCAS}$ | Upper Column Address Strobe |
| $\overline{LCAS}$ | Lower Column Address Strobe |
| $\overline{W}$ | Read/Write Input |
| $\overline{OE}$ | Data Output Enable |
| VCC | Power(+5V) |
| | Power(+3.3V) |
| N.C | No Connection |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Units |
|---|---|---|---|---|
| | | 3.3V | 5V | |
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$,$V_{OUT}$ | -0.5 to +4.6 | -1.0 to +7.0 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | -0.5 to +4.6 | -1.0 to +7.0 | V |
| Storage Temperature | Tstg | -55 to +150 | -55 to +150 | ¡É |
| Power Dissipation | $P_D$ | 1 | 1 | W |
| Short Circuit Output Current | $I_{OS}$ | 50 | 50 | mA |

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, $T_A$= 0 to 70¡É)

| Parameter | Symbol | 3.3V | | | 5V | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{CC}$+0.3*1 | 2.4 | - | $V_{CC}$+1.0*1 | V |
| Input Low Voltage | $V_{IL}$ | -0.3*2 | - | 0.8 | -1.0*2 | - | 0.8 | V |

*1 : $V_{CC}$+1.3V/15ns(3.3V), $V_{CC}$+2.0V/20ns(5V), Pulse width is measured at $V_{CC}$
*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at $V_{SS}$

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

| Max | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| 3.3V | Input Leakage Current (Any input 0¡ÂVIN¡ÂVIN+0.3V, all other input pins not under test=0 Volt) | $I_{I(L)}$ | -5 | 5 | uA |
| | Output Leakage Current (Data out is disabled, 0V¡ÂVOUT¡ÂVCC) | $I_{O(L)}$ | -5 | 5 | uA |
| | Output High Voltage Level($I_{OH}$=-2mA) | $V_{OH}$ | 2.4 | - | V |
| | Output Low Voltage Level($I_{OL}$=2mA) | $V_{OL}$ | - | 0.4 | V |
| 5V | Input Leakage Current (Any input 0¡ÂVIN¡ÂVIN+0.5V, all other input pins not under test=0 Volt) | $I_{I(L)}$ | -5 | 5 | uA |
| | Output Leakage Current (Data out is disabled, 0V¡ÂVOUT¡ÂVCC) | $I_{O(L)}$ | -5 | 5 | uA |
| | Output High Voltage Level($I_{OH}$=-5mA) | $V_{OH}$ | 2.4 | - | V |
| | Output Low Voltage Level($I_{OL}$=4.2mA) | $V_{OL}$ | - | 0.4 | V |

## DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol | Power | Speed | Max | | Units |
|---|---|---|---|---|---|
| | | | KM416V254D | KM416C254D | |
| $I_{CC1}$ | Don't care | -5<br>-6<br>-7 | -<br>70<br>65 | 110<br>90<br>80 | mA<br>mA<br>mA |
| $I_{CC2}$ | Don't care | Don't care | 1 | 2 | mA |
| $I_{CC3}$ | Don't care | -5<br>-6<br>-7 | -<br>70<br>65 | 110<br>90<br>80 | mA<br>mA<br>mA |
| $I_{CC4}$ | Don't care | -5<br>-6<br>-7 | -<br>60<br>55 | 90<br>80<br>70 | mA<br>mA<br>mA |
| $I_{CC5}$ | Normal<br>L | Don't care | 0.5<br>100 | 1<br>150 | mA<br>uA |
| $I_{CC6}$ | Don't care | -5<br>-6<br>-7 | -<br>70<br>65 | 110<br>90<br>80 | mA<br>mA<br>mA |
| $I_{CC7}$ | L | Don't care | 200 | 300 | uA |
| $I_{CCS}$ | L | Don't care | 100 | 200 | uA |

$I_{CC1}$* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

$I_{CC2}$ : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=$V_{IH}$)

$I_{CC3}$* : $\overline{RAS}$-only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=$V_{IH}$, $\overline{RAS}$, Address cycling @tRC=min.)

$I_{CC4}$* : Extended Data Out Mode Current ($\overline{RAS}$=$V_{IL}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

$I_{CC5}$ : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=$V_{CC}$-0.2V)

$I_{CC6}$* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

$I_{CC7}$ : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage($V_{IH}$)=$V_{CC}$-0.2V, Input low voltage($V_{IL}$)=0.2V, $\overline{UCAS}$, $\overline{LCAS}$=0.2V,
Din=Don't care, $T_{RC}$=125us, $T_{RAS}$=$T_{RAS}$min~300ns

$I_{CCS}$ : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$V_{IL}$, $\overline{W}$=$\overline{OE}$=A0 ~ A8=$V_{CC}$-0.2V or 0.2V,
DQ0 ~ DQ15=$V_{CC}$-0.2V, 0.2V or Open

***Note :** $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. $I_{CC}$ is specified as an average current. In $I_{CC1}$, $I_{CC3}$, $I_{CC6}$ and $I_{CC7}$, address can be changed maximum once while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one Hyper page mode cycle time, tHPC.

## CAPACITANCE ($T_A$=25°C, $V_{CC}$=5V or 3.3V, f=1MHz)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input capacitance [A0 ~ A8] | $C_{IN1}$ | - | 5 | pF |
| Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$] | $C_{IN2}$ | - | 7 | pF |
| Output capacitance [DQ0 - DQ15] | $C_{DQ}$ | - | 7 | pF |

## AC CHARACTERISTICS (0°C≤$T_A$≤70°C, See note 1,2)

Test condition (5V device) : $V_{CC}$=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V
Test condition (3.3V device) : $V_{CC}$=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

| Parameter | Symbol | -5 *1 | | -6 | | -7 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | $t_{RC}$ | 84 | | 104 | | 124 | | ns | |
| Read-modify-write cycle time | $t_{RWC}$ | 116 | | 138 | | 163 | | ns | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | | 50 | | 60 | | 70 | ns | 3,4,10 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | | 15 | | 15 | | 20 | ns | 3,4,5 |
| Access time from column address | $t_{AA}$ | | 25 | | 30 | | 35 | ns | 3,10 |
| $\overline{CAS}$ to output in Low-Z | $t_{CLZ}$ | 3 | | 3 | | 3 | | ns | 3 |
| Output buffer turn-off dealy from $\overline{CAS}$ | $t_{CEZ}$ | 3 | 13 | 3 | 13 | 3 | 18 | ns | 6,13 |
| Transition time (rise and fall) | $t_T$ | 2 | 50 | 2 | 50 | 2 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 30 | | 40 | | 50 | | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 50 | 10K | 60 | 10K | 70 | 10K | ns | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | | 15 | | 20 | | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 40 | | 50 | | 60 | | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 8 | 10K | 10 | 10K | 15 | 10K | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 35 | 20 | 45 | 20 | 50 | ns | 4 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 25 | 15 | 30 | 15 | 35 | ns | 10 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | | 5 | | 5 | | ns | |
| Row address set-up time | $t_{ASR}$ | 0 | | 0 | | 0 | | ns | |
| Row address hold time | $t_{RAH}$ | 10 | | 10 | | 10 | | ns | |
| Column address set-up time | $t_{ASC}$ | 0 | | 0 | | 0 | | ns | 14 |
| Column address hold time | $t_{CAH}$ | 8 | | 10 | | 15 | | ns | 14 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 25 | | 30 | | 35 | | ns | |
| Read command set-up time | $t_{RCS}$ | 0 | | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | | 0 | | 0 | | ns | 8 |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | | 0 | | 0 | | ns | 8 |
| Write command set-up time | $t_{WCS}$ | 0 | | 0 | | 0 | | ns | 7 |
| Write command hold time | $t_{WCH}$ | 10 | | 10 | | 10 | | ns | |
| Write command pulse width | $t_{WP}$ | 10 | | 10 | | 10 | | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 13 | | 15 | | 15 | | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 8 | | 10 | | 15 | | ns | 17 |

Note) *1 : 5V only

## AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -5 *1 | | -6 | | -7 | | Units | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Data set-up time | $t_{DS}$ | 0 | | 0 | | 0 | | ns | 9,20 |
| Data hold time | $t_{DH}$ | 8 | | 10 | | 15 | | ns | 9,20 |
| Refresh period (Normal) | $t_{REF}$ | | 8 | | 8 | | 8 | ms | |
| Refresh period (L-ver) | $t_{REF}$ | | 128 | | 128 | | 128 | ms | |
| $\overline{CAS}$ to $\overline{W}$ delay time | $t_{CWD}$ | 32 | | 32 | | 42 | | ns | 7,16 |
| $\overline{RAS}$ to $\overline{W}$ delay time | $t_{RWD}$ | 67 | | 77 | | 92 | | ns | 7 |
| Column address to $\overline{W}$ delay time | $t_{AWD}$ | 42 | | 47 | | 57 | | ns | 7 |
| $\overline{CAS}$ precharge to $\overline{W}$ delay time | $t_{CPWD}$ | 45 | | 52 | | 62 | | ns | 7 |
| $\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh) | $t_{CSR}$ | 5 | | 5 | | 5 | | ns | 18 |
| $\overline{CAS}$ hlod time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh) | $t_{CHR}$ | 10 | | 10 | | 10 | | ns | 19 |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $t_{RPC}$ | 5 | | 5 | | 5 | | ns | |
| $\overline{CAS}$ precharge time (CBR counter test cycle) | $t_{CPT}$ | 20 | | 20 | | 25 | | ns | |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | | 28 | | 35 | | 40 | ns | 3 |
| Hyper Page mode cycle time | $t_{HPC}$ | 20 | | 25 | | 30 | | ns | 11 |
| Hyper Page read-modify-write cycle time | $t_{HPRWC}$ | 57 | | 66 | | 81 | | ns | 11 |
| $\overline{CAS}$ precharge time (Hyper Page cycle) | $t_{CP}$ | 8 | | 10 | | 10 | | ns | 15 |
| $\overline{RAS}$ pulse width (Hyper Page cycle) | $t_{RASP}$ | 50 | 100K | 60 | 100K | 70 | 100K | ns | |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{RHCP}$ | 30 | | 35 | | 40 | | ns | |
| $\overline{OE}$ access time | $t_{OEA}$ | | 15 | | 15 | | 20 | ns | 3 |
| $\overline{OE}$ to data delay | $t_{OED}$ | 13 | | 13 | | 18 | | ns | |
| Output buffer turn off delay time from $\overline{OE}$ | $t_{OEZ}$ | 3 | 13 | 3 | 13 | 3 | 18 | ns | 6 |
| $\overline{OE}$ command hold time | $t_{OEH}$ | 15 | | 15 | | 20 | | ns | |
| Output data hold time | $t_{DOH}$ | 5 | | 5 | | 5 | | ns | |
| Output buffer turn off delay from $\overline{RAS}$ | $t_{REZ}$ | 3 | 15 | 3 | 15 | 3 | 20 | ns | 6,13 |
| Output buffer turn off delay from $\overline{W}$ | $t_{WEZ}$ | 3 | 13 | 3 | 13 | 3 | 18 | ns | 6 |
| $\overline{W}$ to data delay | $t_{WED}$ | 13 | | 13 | | 18 | | ns | |
| $\overline{OE}$ to $\overline{CAS}$ hold time | $t_{OCH}$ | 5 | | 5 | | 5 | | ns | |
| $\overline{CAS}$ hold time to $\overline{OE}$ | $t_{CHO}$ | 5 | | 5 | | 5 | | ns | |
| $\overline{OE}$ precharge time | $t_{OEP}$ | 5 | | 5 | | 5 | | ns | |
| $\overline{W}$ pulse width (Hyper Page Cycle) | $t_{WPE}$ | 5 | | 5 | | 5 | | ns | |
| $\overline{RAS}$ pulse width (C-B-R self refresh) | $t_{RASS}$ | 100 | | 100 | | 100 | | us | 12 |
| $\overline{RAS}$ precharge time (C-B-R self refresh) | $t_{RPS}$ | 90 | | 110 | | 130 | | ns | 12 |
| $\overline{CAS}$ hold time (C-B-R self refresh) | $t_{CHS}$ | -50 | | -50 | | -50 | | ns | 12 |

Note) *1 : 5V only

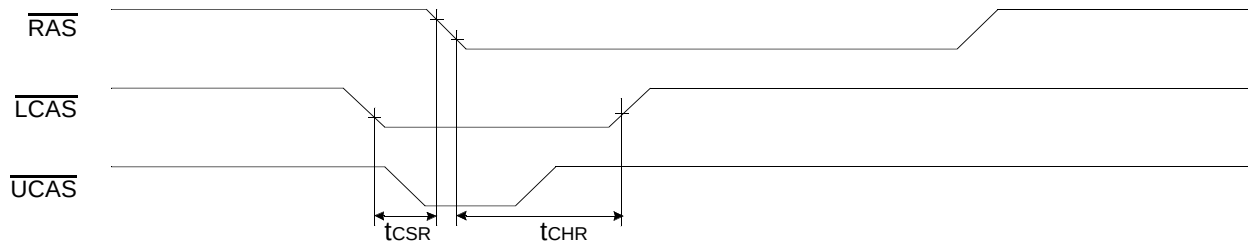
## NOTES

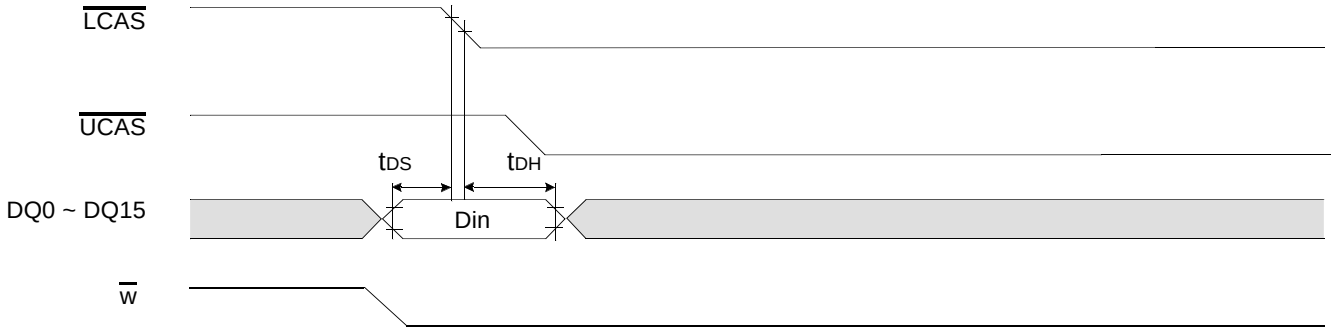
1. An initial pause of 200us is required after power-up followed by any 8 ROR or $\overline{CBR}$ cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 50pF.
4. Operation within the $t_{RCD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RCD}$(max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.
5. Assumes that $t_{RCD} \leq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to $V_{oh}$ or $V_{ol}$.
7. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in ealy write cycles and to the $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{RAD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RAD}$(max) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit, then access time is controlled by $t_{AA}$.
11. $t_{ASC} \geq$ 6ns, Assume tT = 2.0ns
12. 512cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).

### KM416C/V254D/DL Truth Table

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{W}$ | $\overline{OE}$ | DQ0 - DQ7 | DQ8-DQ15 | STATE |
|---|---|---|---|---|---|---|---|
| H | H | H | H | H | Hi-Z | Hi-Z | Standby |
| L | H | H | H | H | Hi-Z | Hi-Z | Refresh |
| L | L | H | H | L | DQ-OUT | Hi-Z | Byte Read |
| L | H | L | H | L | Hi-Z | DQ-OUT | Byte Read |
| L | L | L | H | L | DQ-OUT | DQ-OUT | Word Read |
| L | L | H | L | H | DQ-IN | - | Byte Write |
| L | H | L | L | H | - | DQ-IN | Byte Write |
| L | L | L | L | H | DQ-IN | DQ-IN | Word Write |
| L | L | L | H | H | Hi-Z | Hi-Z | - |

13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ rising edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word red-modify-write cycle.
17. $t_{CWL}$ is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
18. $t_{CSR}$ is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. $t_{CHR}$ is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.




20. $t_{DS}$, $t_{DH}$ are specified for the earlier $\overline{CAS}$ falling low.