256K x 16 EDO DRAM
5.0 Volt, 125 MHz

Features

- 262,144-Word by 16-Bit organization
- Single +5.0V ± 10% power supply
- 512 refresh cycles / 8 ms
- Refresh modes: RAS-only, CAS-before-RAS (CBR) and Hidden
- Dual CAS for Byte Write and Byte Read control
- Fast Page Mode with Extended Data Out (EDO)
- JEDEC standard 400 mil, 40-pin SOJ and 44-pin TSOP II packages

Description

The SM81C256K16C is a high-speed randomly accessed memory for graphics, organized in a 262,144-word by 16-bit configuration. This product can execute Byte Write and Byte Read operation via two CAS pins.

The SM81C256K16C offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO). This allows random access of up to 512 (x16) words within a row at a 125-MHz EDO cycle, making the SM81C256K16C ideally suited for graphics, digital signal processing and high performance computing systems.

Key Timing Parameters

SM81C256K16C	- 8 (125 MHz)
Min. EDO Cycle Time (t_{PC})	8 ns
Max. Access Time from CAS (t_{CAC})	8 ns
Max. Access Time from Column Address (t_{AA})	11 ns

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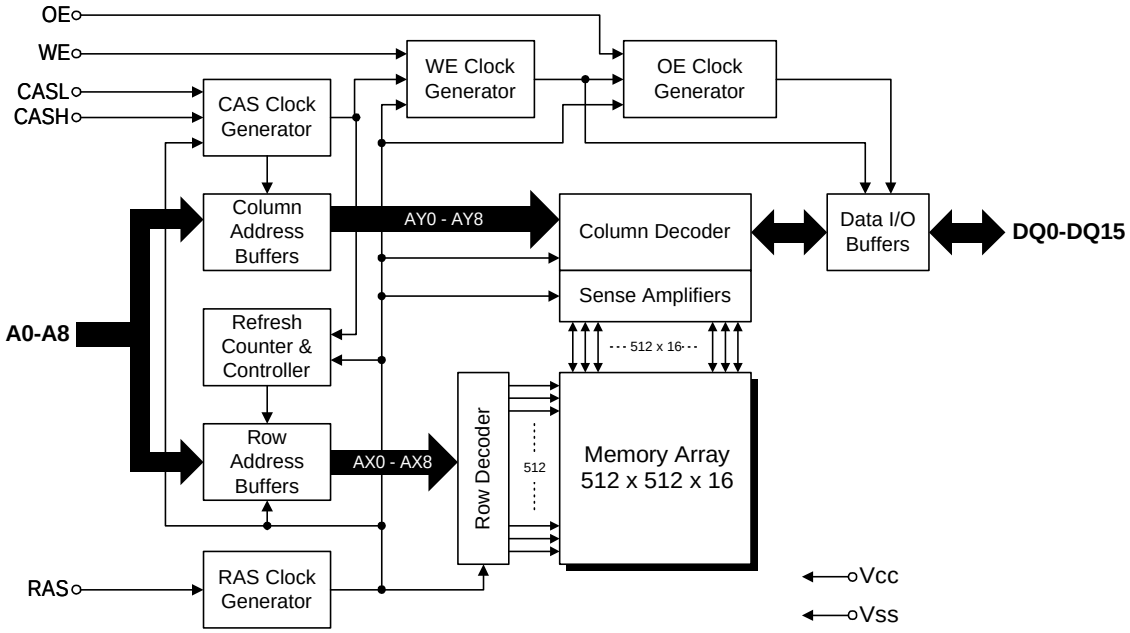
Ordering Information

Part Number	Speed Grade	Package
SM81C256K16CJ-8	125 MHz	40-pin SOJ
SM81C256K16CS-8	125 MHz	44-pin TSOP

Functional Block Diagram



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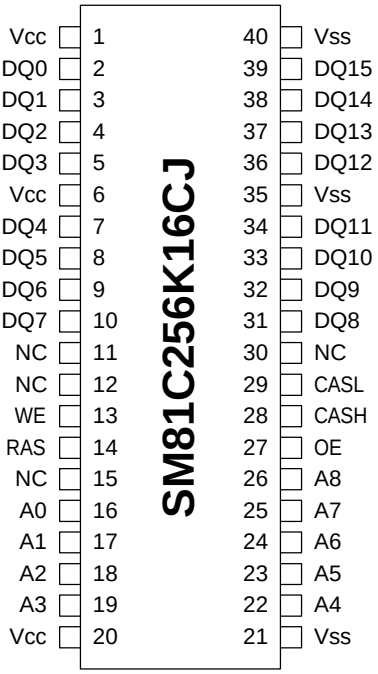
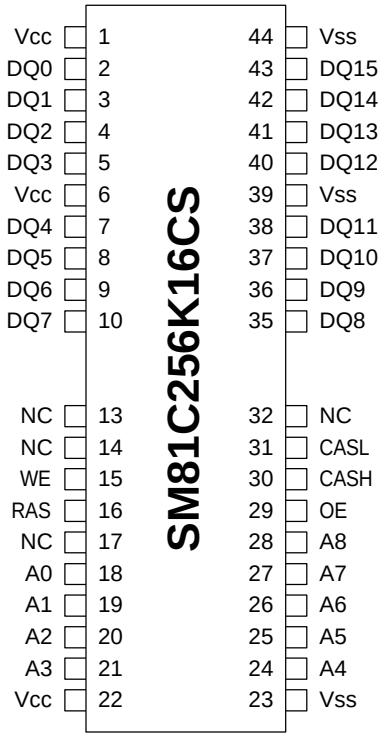
Pin Assignment (Top View)

40-pin SOJ



44-pin TSOP II



Pin Descriptions

Pin Name	Description
A0 - A8	Address Inputs
RAS	Row Address Strobe
CASL	Column Address Strobe for Lower Byte (DQ0 - DQ7)
CASH	Column Address Strobe for Upper Byte (DQ8 - DQ15)
WE	Write Enable
OE	Output Enable
DQ0 - DQ15	Data Input / Output
Vcc	+5V Supply
Vss	Ground
NC	No Connection: This pin should be left unconnected or tied to ground.

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Functional Description

The SM81C256K16C reads and writes data by multiplexing an 18-bit address into a 9-bit row and 9-bit column address. RAS and CAS are used to strobe the row address and the column address, respectively.

The SM81C256K16C has two CAS inputs: CASL controls DQ0 - DQ7, and CASH controls DQ8 - DQ15. CASL and CASH function in an identical manner to CAS in that either will generate an internal CAS signal. The CAS function and timing are determined by the first CAS (CASL or CASH) to transition low and by the last to transition high. Byte Read and Byte Write are controlled by using CASL and CASH separately.

A Read cycle is performed by holding the WE signal high during RAS/CAS operation. A Write cycle is executed by holding the WE signal low during RAS/CAS operation; the input data is latched by the falling edge of WE or CAS, whichever occurs later. The data inputs and outputs are routed through 16 common I/O pins, with RAS, CAS, WE and OE controlling the pin direction.

Fast Page Mode operation permits all 512 columns within a selected row to be randomly accessed at a high data rate. A Fast Page Mode cycle is initiated with a row address latched by RAS followed by a column address latched by CAS. While holding RAS low, CAS can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

The SM81C256K16C offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the CAS precharge time (t_{CP}). Since data can be output after CAS goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain valid as long as RAS and OE are low, and WE is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Mode Read.

A memory cycle is terminated by returning both RAS and CAS high. Memory cell data will retain its correct state by maintaining power and accessing all 512 combinations of the 9-bit row addresses, regardless of sequence, at least once every 8ms through any RAS cycle (Read, Write) or RAS Refresh cycle (RAS-only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

Power-Up Sequence

The initial application of the Vcc supply requires a 200-µs wait followed by a minimum of any eight initialization cycles containing a RAS clock. During Power-Up, the Vcc current is dependent on the input levels of RAS and CAS. It is recommended that RAS and CAS track with Vcc or be held at a valid V_{IH} during Power-Up to avoid current surges.

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Truth Table

(X = Don't Care)

Function	RAS	CASL	CASH	WE	OE	Address	DQ0 – DQ15	Notes
Standby	H	H	H	X	X	X	High-Z	
Read: Word	L	L	L	H	L	Row/Col.	Data Out	
Read: Lower Byte	L	L	H	H	L	Row/Col.	DQ0-7 = Data Out DQ8-15 = High-Z	
Read: Upper Byte	L	H	L	H	L	Row/Col.	DQ0-7 = High-Z DQ8-15 = Data Out	
Write: Word (Early)	L	L	L	L	X	Row/Col.	Data In	
Write: Lower Byte (Early)	L	L	H	L	X	Row/Col.	DQ0-7 = Data In DQ8-15 = X	
Write: Upper Byte (Early)	L	H	L	L	X	Row/Col.	DQ0-7 = X DQ8-15 = Data In	
Read-Write	L	L	L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
Fast-Page-Mode Read: EDO								
- First cycle	L	H→L	H→L	H	L	Row/Col.	Data Out	2
- Subsequent cycles	L	H→L	H→L	H	L	Col.	Data Out	2
Fast-Page-Mode Read: Hi-Z								
- First cycle	L	H→L	H→L	H	H→L	Row/Col.	Data Out	2
- Subsequent cycles	L	H→L	H→L	H	H→L	Col.	Data Out	2
Fast-Page-Mode Write (Early)								
- First cycle	L	H→L	H→L	L	X	Row/Col.	Data In	1
- Subsequent cycles	L	H→L	H→L	L	X	Col.	Data In	1
Fast-Page-Mode Read-Write								
- First cycle	L	H→L	H→L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
- Subsequent cycles	L	H→L	H→L	H→L	L→H	Col.	Data Out → Data In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	Row/Col.	Data Out	2
Hidden Refresh Write	L→H→L	L	L	L	X	Row/Col.	Data In → High-Z	1
RAS-Only Refresh	L	H	H	X	X	Row	High-Z	
CBR Refresh	H→L	L	L	X	X	X	High-Z	3

Note:

1. Byte Write may be executed with either CASL or CASH active.
2. Byte Read may be executed with either CASL or CASH active.
3. Only one CAS signal (CASL or CASH) must be active.

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Electrical Characteristics

*Absolute Maximum Ratings**

Ambient Temperature Under Bias..... -1.0 °C to +80 °C
Storage Temperature ..... -50 °C to 125 °C
Voltage Relative to Vss ..... -1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation..... 1.5 W

* Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions

(T_A = 0 °C to 70 °C)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	3.0	—	V_{CC} + 1.0	V	1
Input Low Voltage	V_{IL}	-0.5	—	0	V	1

*Capacitance**

(V_{CC} = 5V, T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Maximum	Unit
Input Capacitance	C_{IN}	5	pF
Input/Output Capacitance	C_{IO}	7	pF

* Note: Capacitance is sampled and not 100% tested.

DC Characteristics

(Note: 1, V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Parameter	Symbol	Condition	-8 (125 MHz) Min.	-8 (125 MHz) Max.	Unit	Notes
Input High (Logic 1) Voltage, all inputs	V_{IH}		2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}		-0.5	0.8	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}	-10	10	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 5.5V; outputs disabled	-10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	RAS, CAS = cycling; t_{RC} = Min.	-	260	mA	2, 3, 15, 16
Power Supply Current (Standby)	I_{CC2}	RAS, CAS = V_{IH}	-	2	mA	
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	RAS = cycling; CAS = V_{IH}; t_{RC} = Min.	-	260	mA	2, 3, 15, 16
Average Power Supply Current (Fast Page Mode)	I_{CC4}	RAS = V_{IL}; CAS = cycling; t_{PC} = Min.	-	200	mA	2, 3, 15, 18
Average Power Supply Current (CAS-before-RAS Refresh)	I_{CC5}	RAS = cycling; CAS before RAS	-	260	mA	2, 3, 15, 16

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AC Characteristics

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Parameter	Symbol	-8 (125 MHz)		Unit	Notes
		Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	45		ns	
Read Modify Write Cycle Time	t_{RMW}	65		ns	
EDO Cycle Time	t_{PC}	8		ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRMW}	32		ns	
Access Time from RAS	t_{RAC}		24	ns	7, 12, 13
Access Time from Column Address	t_{AA}		11	ns	7, 13
Access Time from CAS	t_{CAC}		8	ns	7, 12
Access Time from CAS Precharge	t_{CPA}		12	ns	7, 12
Output Buffer Turn-Off Delay Time from RAS	t_{REZ}	3	6	ns	8
Output Buffer Turn-Off Delay Time from CAS	t_{CEZ}	3	6	ns	8
Transition Time (Rise and Fall)	t_T	0.5	35	ns	6
RAS Precharge Time	t_{RP}	15		ns	
RAS Pulse Width	t_{RAS}	25	10k	ns	
RAS Pulse Width (Fast Page Mode Only)	t_{RASP}	25	100k	ns	
RAS Hold Time	t_{RSH}	7		ns	
CAS Hold Time	t_{CSH}	20		ns	
CAS Pulse Width	t_{CAS}	3	10k	ns	
RAS to CAS Delay Time	t_{RCD}	10	16	ns	12
RAS to Column Address Delay Time	t_{RAD}	8	13	ns	13
Column Address to RAS Lead Time	t_{RAL}	11		ns	
CAS to RAS Precharge Time	t_{CRP}	5		ns	
CAS Precharge Time (Fast Page Mode)	t_{CP}	3		ns	
Row Address Set-Up Time	t_{ASR}	0		ns	
Row Address Hold Time	t_{RAH}	6		ns	
Column Address Set-Up Time	t_{ASC}	0		ns	
Column Address Hold Time	t_{CAH}	4		ns	
Column Address Hold Time referenced to RAS	t_{AR}	19		ns	
Read Command Set-Up Time	t_{RCS}	0		ns	

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AC Characteristics (continued)

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Parameter	Symbol	-8 (125 MHz)		Unit	Notes
		Min.	Max.		
Read Command Hold Time referenced to CAS	tRCH	0		ns	9
Read Command Hold Time referenced to RAS	tRRH	0		ns	9
CAS "H" to RAS "H" Lead Time	tCRL	0		ns	
RAS "H" to CAS "H" Lead Time	tRCL	0		ns	
Data Output Hold after CAS low	tDOH	3		ns	17
Write Command Set-Up Time	tWCS	0		ns	11
Write Command Hold Time	tWCH	5		ns	
Write Command Hold Time referenced to RAS	tWCR	19		ns	
Write Command Pulse Width	tWP	5		ns	
Write Command to RAS Lead Time	tRWL	7		ns	
Write Command to CAS Lead Time	tCWL	5		ns	
Output Buffer Turn-Off Delay Time from WE	tWEZ	3	6	ns	8
Data Set-Up Time	tDS	0		ns	10
Data Hold Time	tDH	5		ns	10
Data Hold Time referenced to RAS	tDHR	19		ns	
RAS to WE Delay Time	tRWD	31		ns	11
Column Address to WE Delay Time	tAWD	19		ns	11
CAS to WE Delay Time	tCWD	16		ns	11
Access Time from OE	tOEA		8	ns	
Output Buffer Turn-Off Delay Time from OE	tOEZ	3	6	ns	8
OE to Data Delay Time	tOED	7		ns	
OE Command Hold Time	tOEH	5		ns	
RAS Hold Time referenced to OE	tROH	7		ns	
OE "L" to CAS "H" Lead Time	tOCH	5		ns	
CAS "H" to OE "L" Lead Time	tCHO	5		ns	
Hi-Z Command Pulse Width	tOEP	5		ns	
CAS Set-Up Time for CAS-before-RAS Cycle	tCSR	5		ns	
CAS Hold Time for CAS-before-RAS Cycle	tCHR	7		ns	
RAS Precharge to CAS Active Time	tRPC	0		ns	
Refresh Period	tREF		8	ms	

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Notes

1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200µs is required after power-up followed by any eight RAS cycles (example: RAS-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight CAS-before-RAS cycles instead of eight RAS cycles are required.
5. The AC characteristics assume at t_T = 1.0 ns.
6. $V_{IH(min.)}$ and $V_{IL(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 50pF. DOUT reference levels: V_{OH}/V_{OL} = 1.6V/1.4V.
8. $t_{REZ(max.)}$, $t_{CEZ(max.)}$, $t_{WEZ(max.)}$, and $t_{OEZ(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to CAS leading edge of early Write cycles and to WE leading edge in OE-controlled Write cycles and Read-Modify-Write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early Write cycle, and the data out pins will remain tri-state throughout the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, and $t_{AWD} \geq t_{AWD(min.)}$, the cycle is a Read-Modify-Write cycle, and the output data will contain data read from the addresssed memory cells. If neither of the above sets of conditions is satisfied, the condition of the output data is indeterminate.
12. Operation within the $t_{RCD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
13. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0-A8) may be changed at most two times while RAS = V_{IL}.
16. Addresses (A0-A8) may be changed at most once while CAS = V_{IH} and RAS = V_{IL}.
17. This is guaranteed by design. (t_{DOH} = t_{CAC} – output transition time). This parameter is not 100% tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

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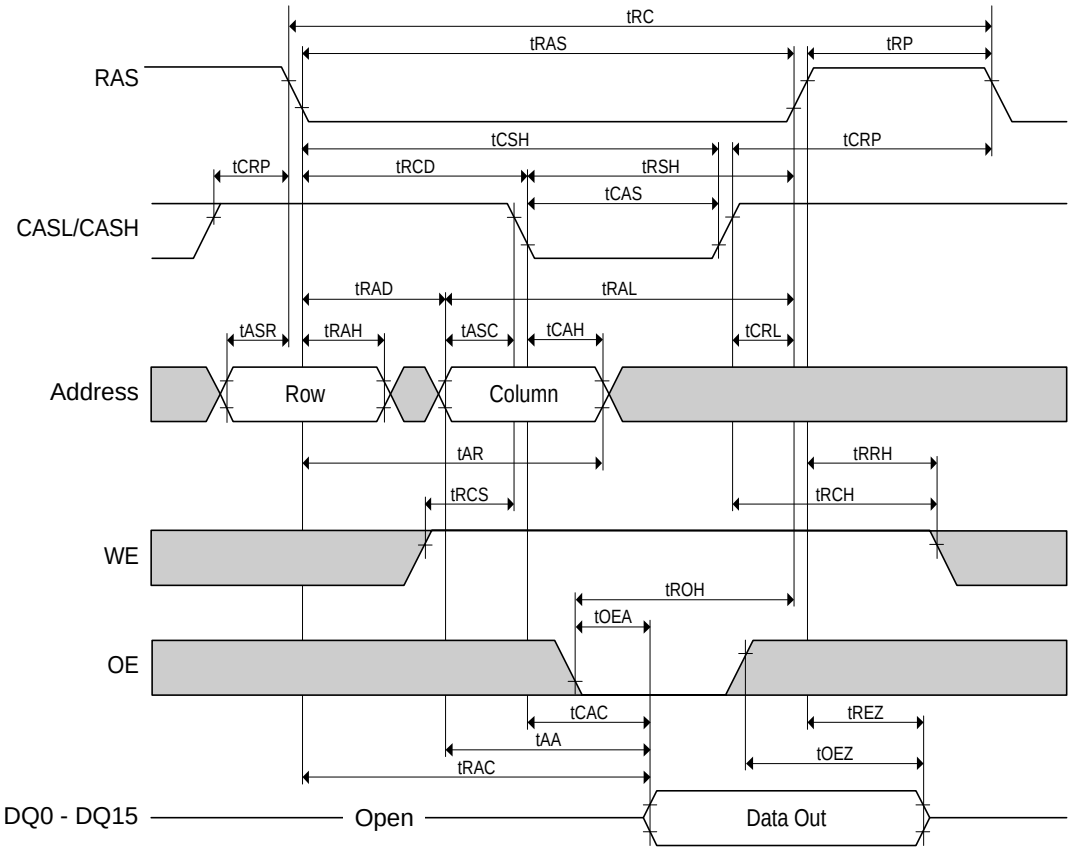
Read Cycle (Outputs Controlled by RAS)



: "H" or "L"

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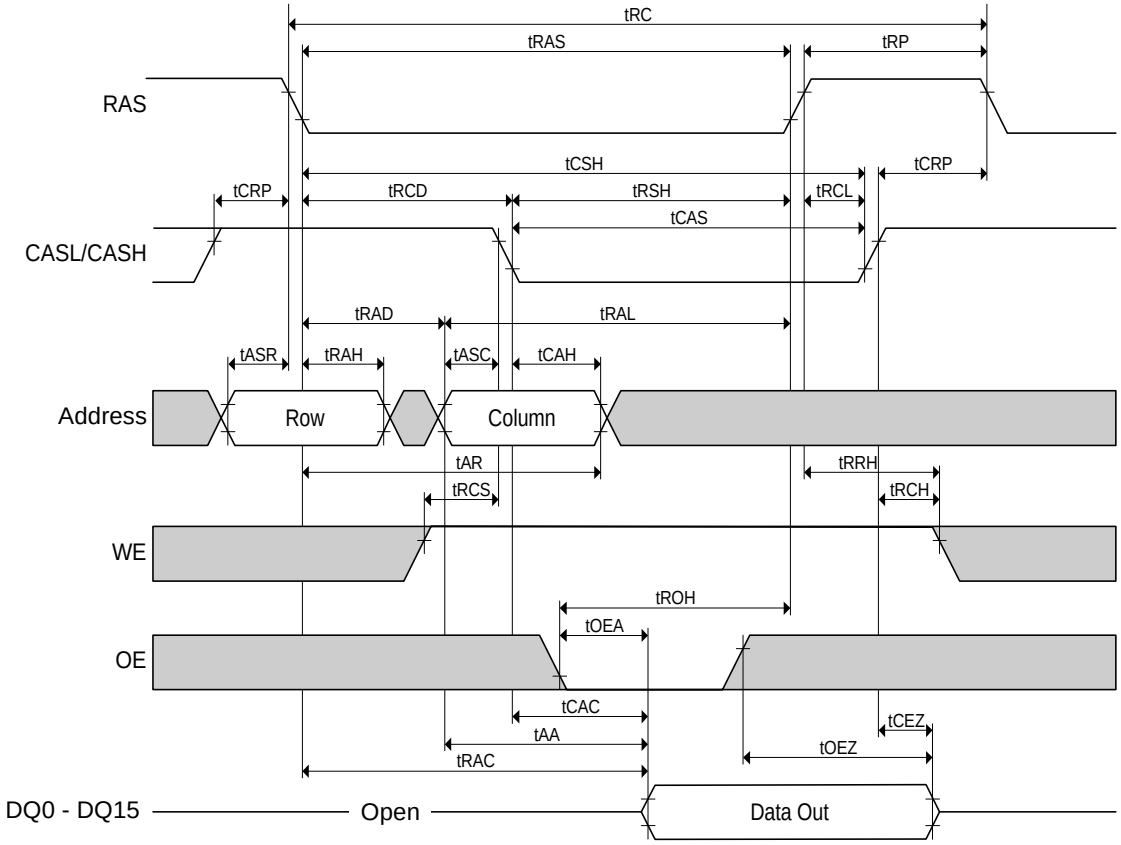
Read Cycle (Outputs Controlled by CAS)



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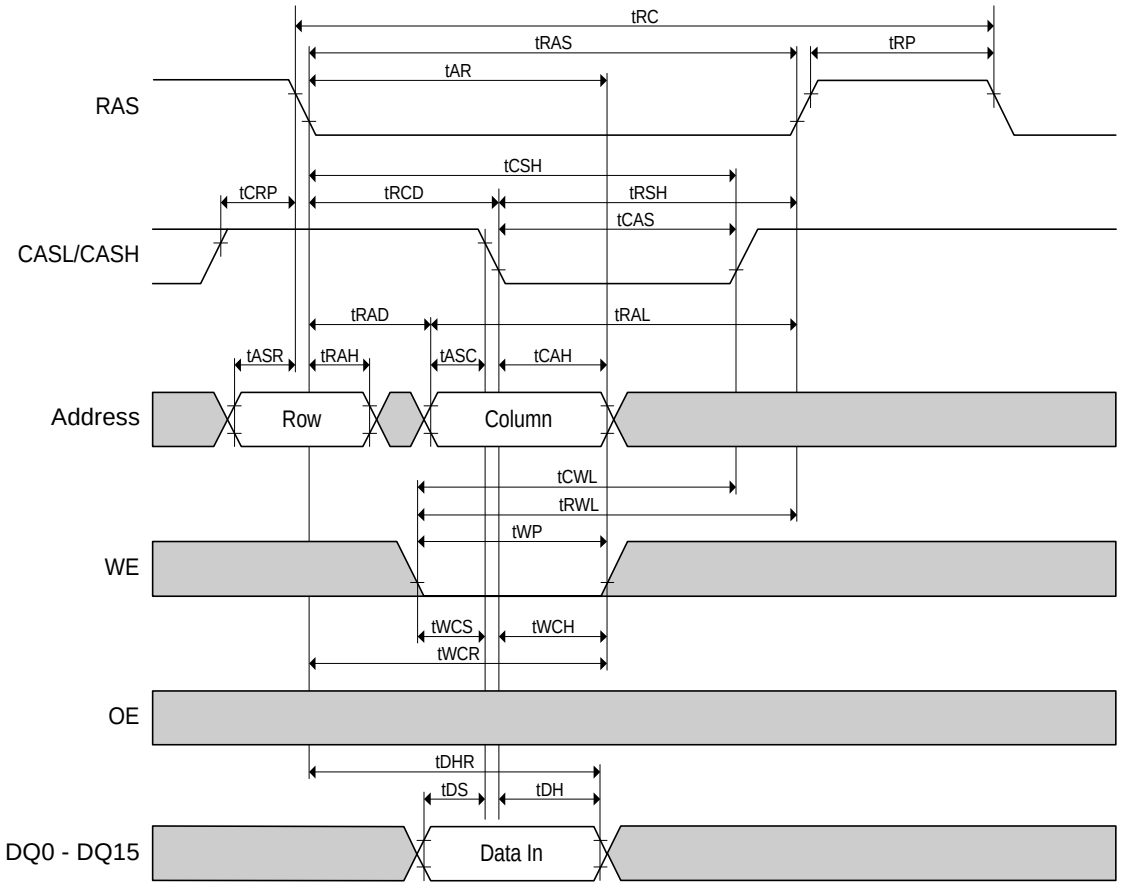
Write Cycle (Early Write)



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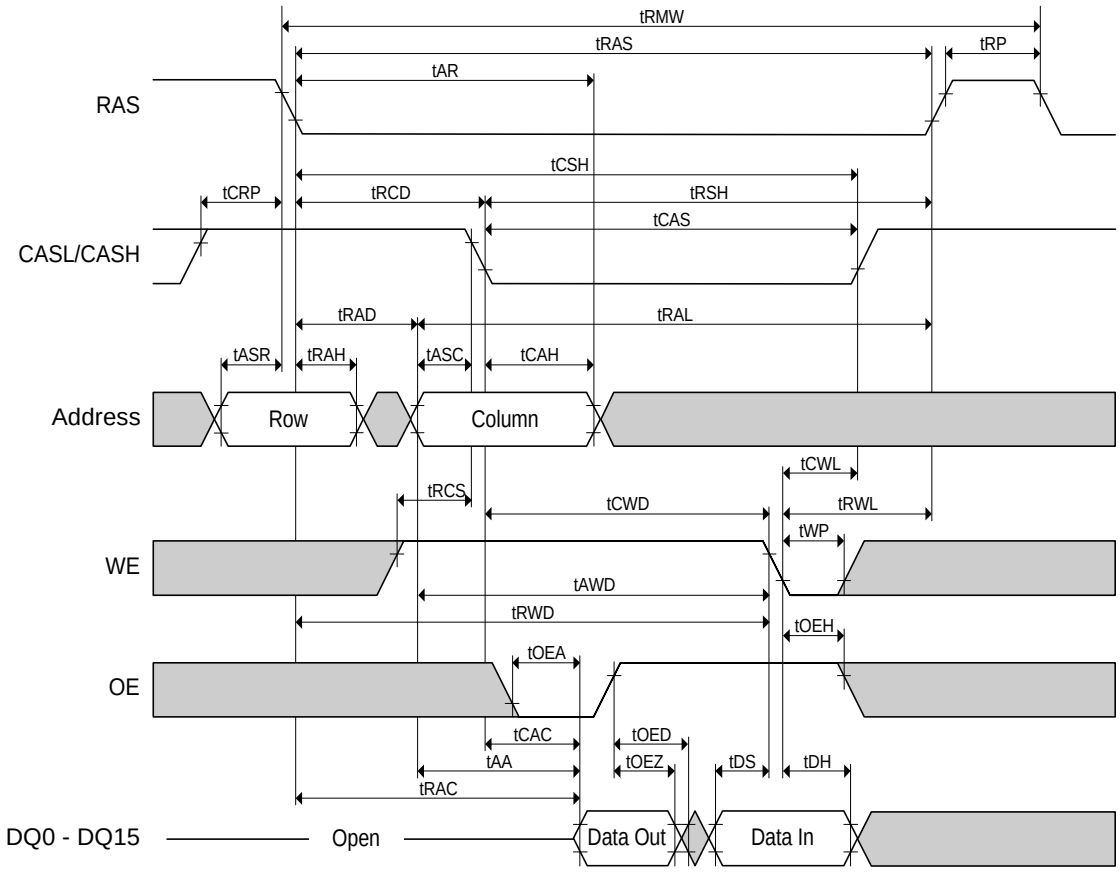
Read-Modify-Write Cycle



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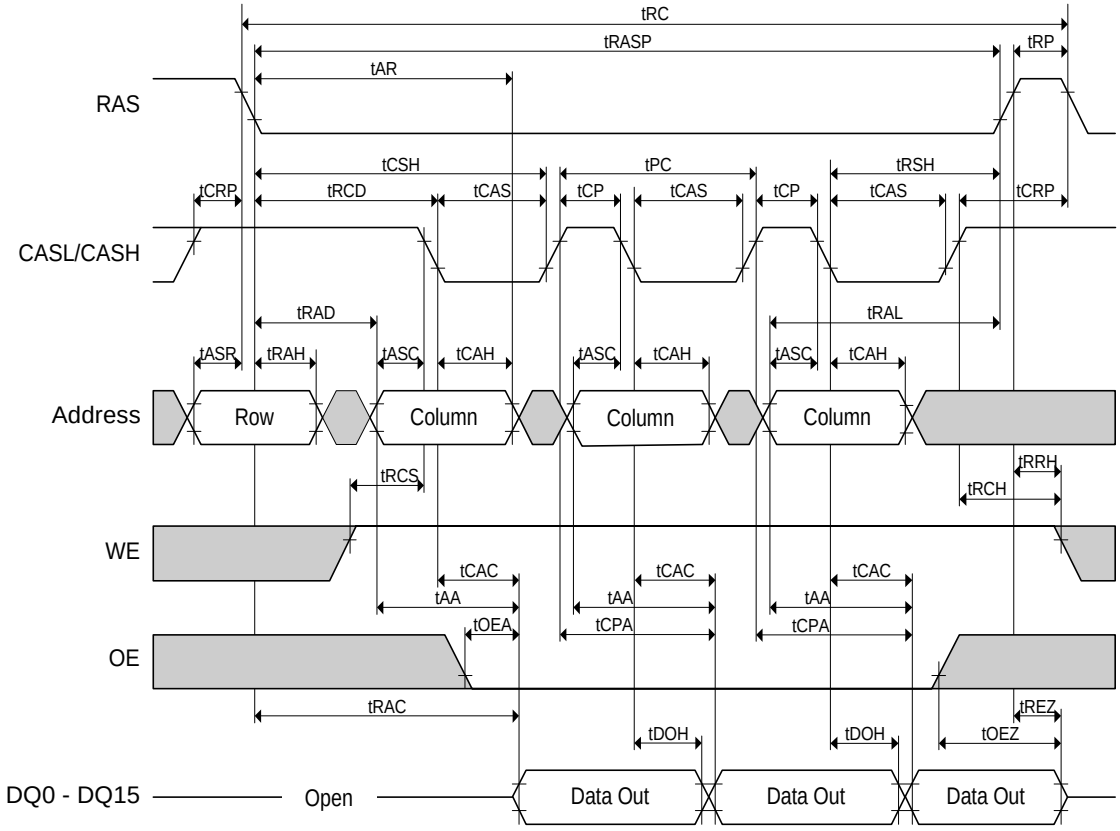
Fast-Page-Mode Read Cycle with Extended Data Out



: "H" or "L"

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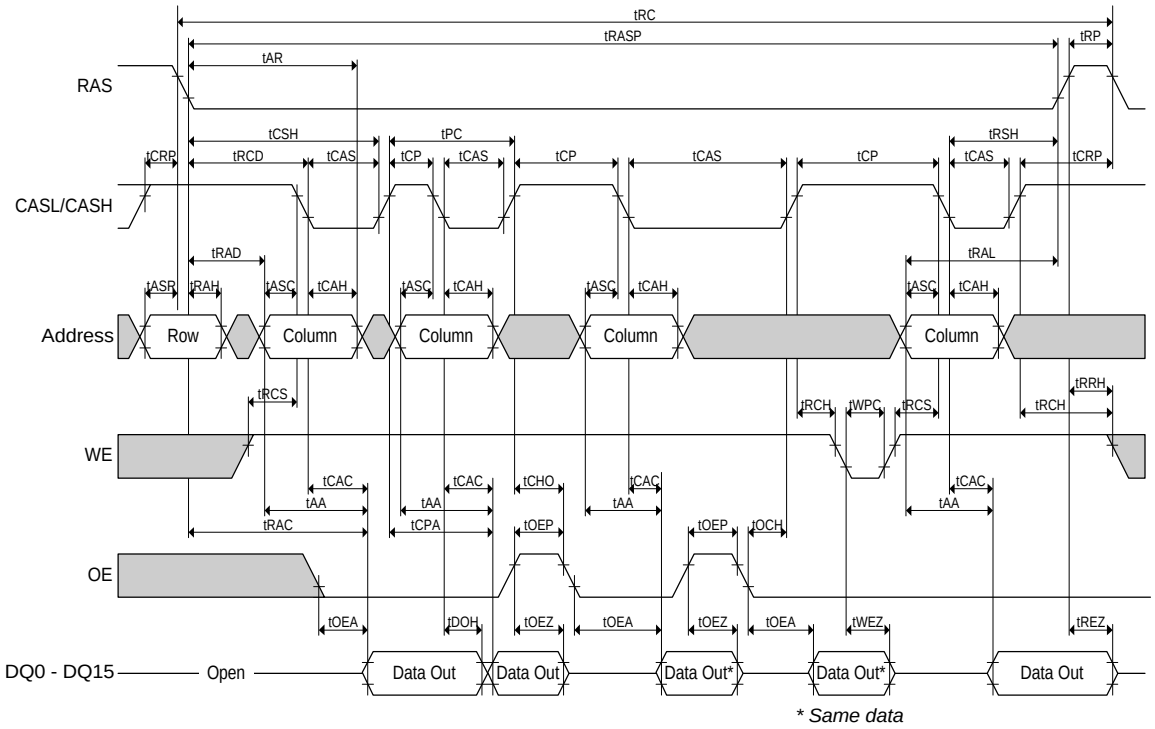
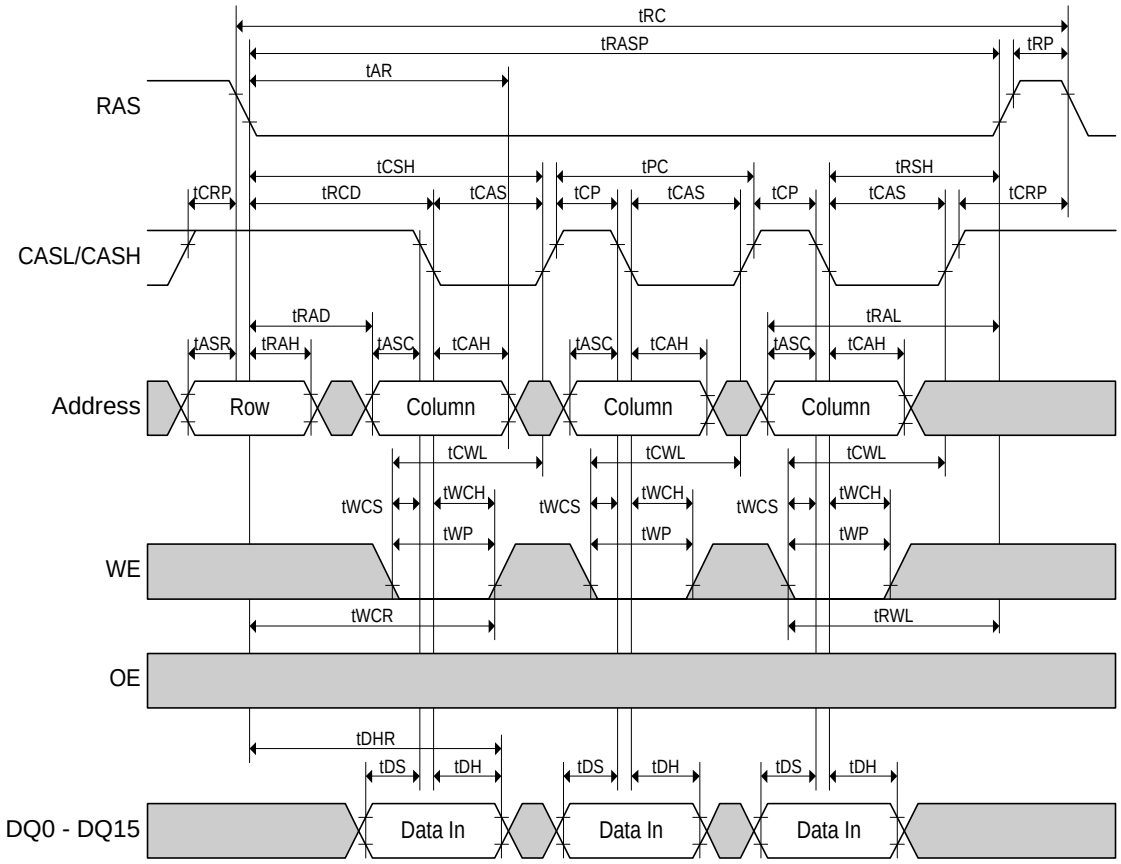
Fast-Page-Mode Read Cycle with Hi-Z Operation



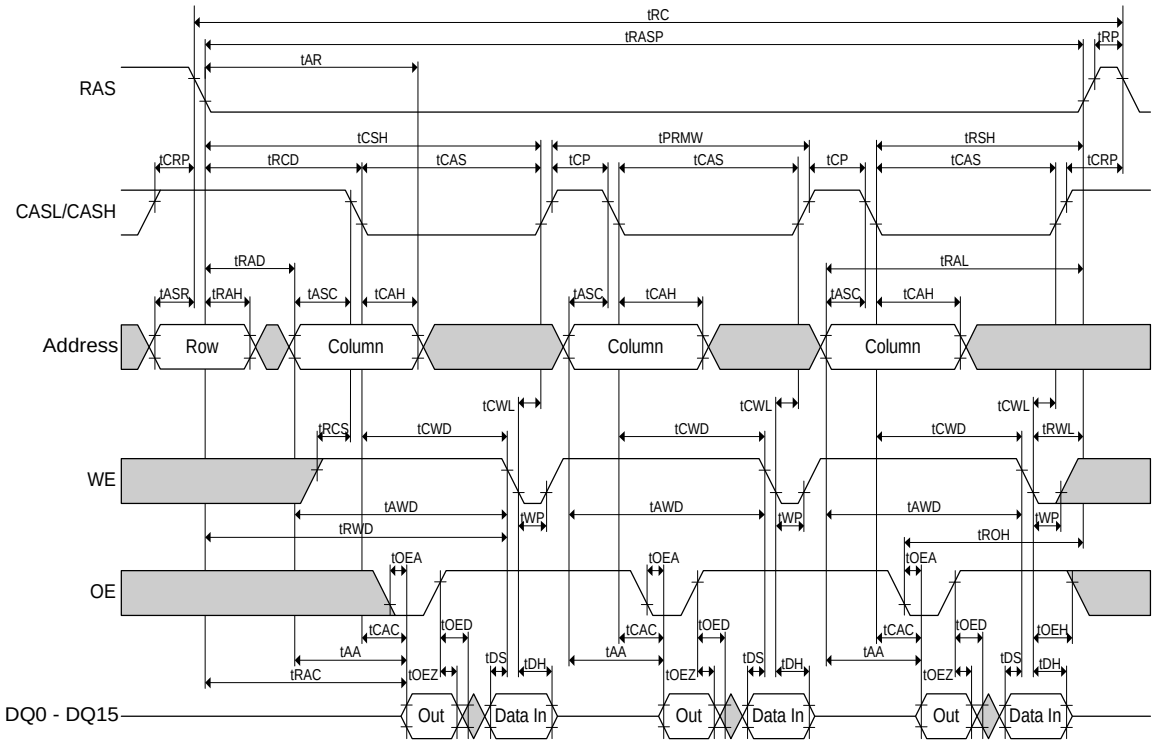
: "H" or "L"

Fast-Page-Mode Write Cycle (Early Write)



: "H" or "L"

Fast-Page-Mode Read-Modify-Write Cycle



: "H" or "L"

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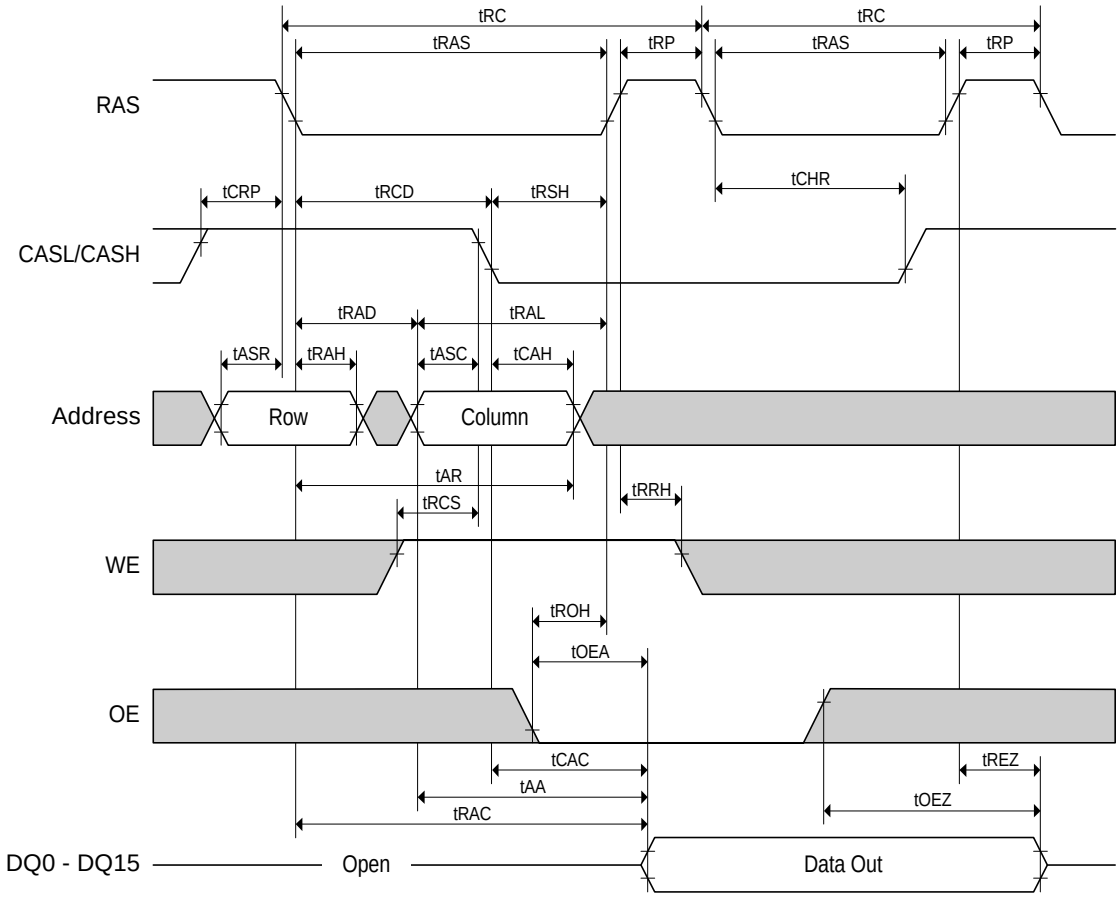
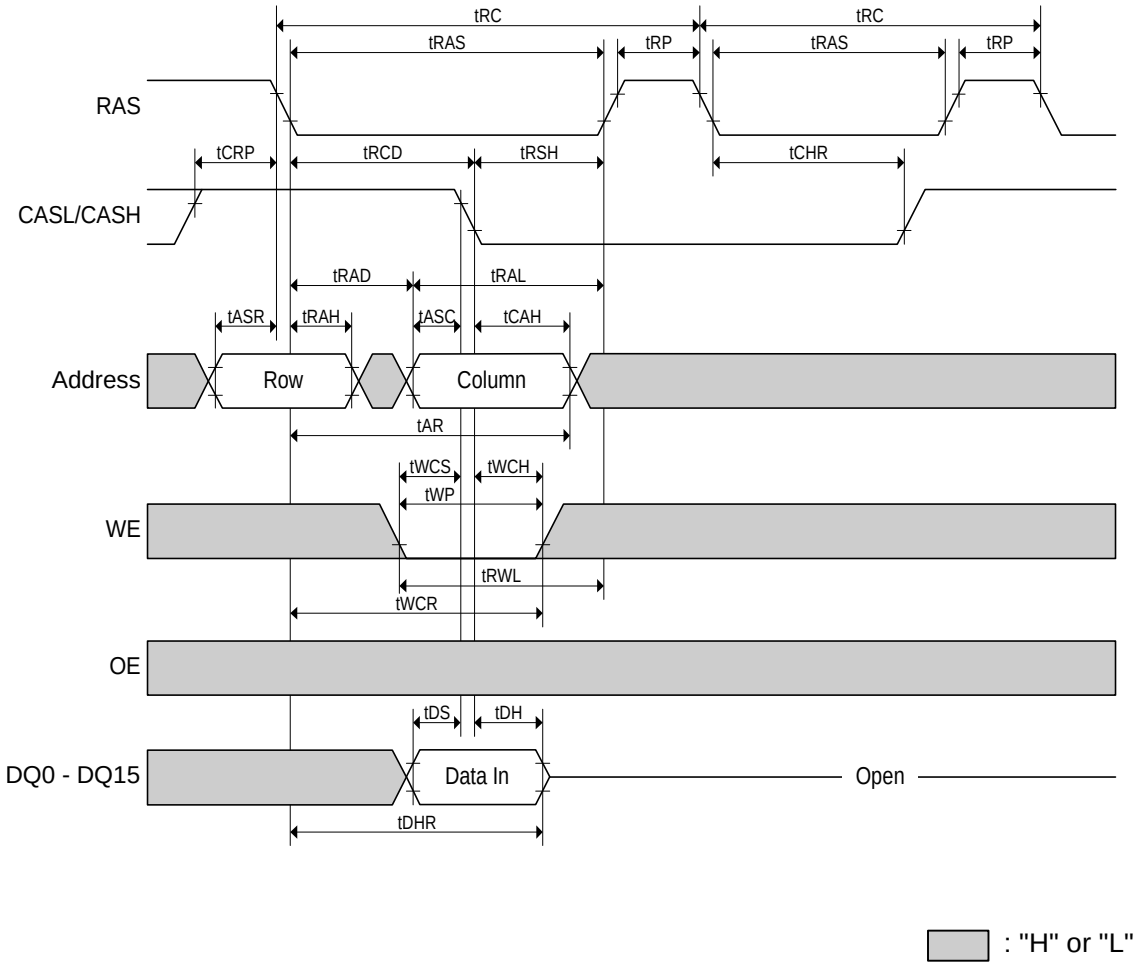
Hidden Refresh Read Cycle



: "H" or "L"

Hidden Refresh Write Cycle



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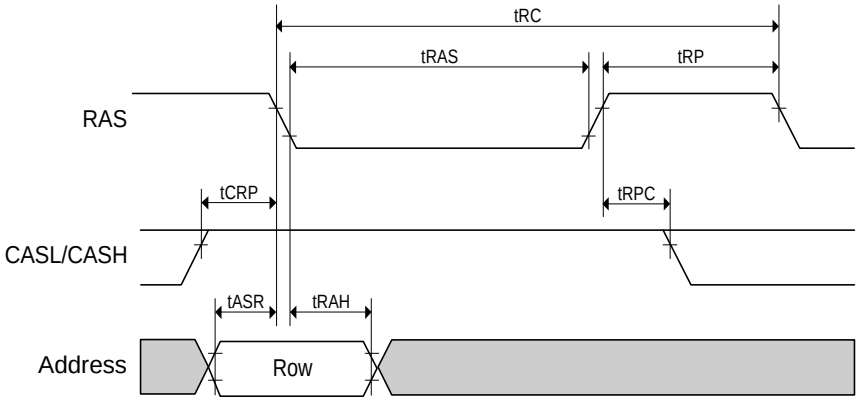
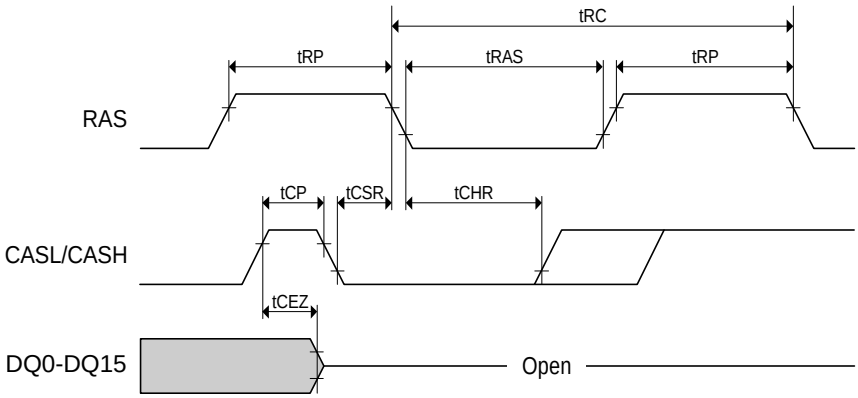
RAS-Only Refresh Cycle



Note: DQ's are open; WE and OE = "H" or "L"

CAS-Before-RAS Refresh Cycle



Note: WE, OE and Address = "H" or "L".

: "H" or "L"

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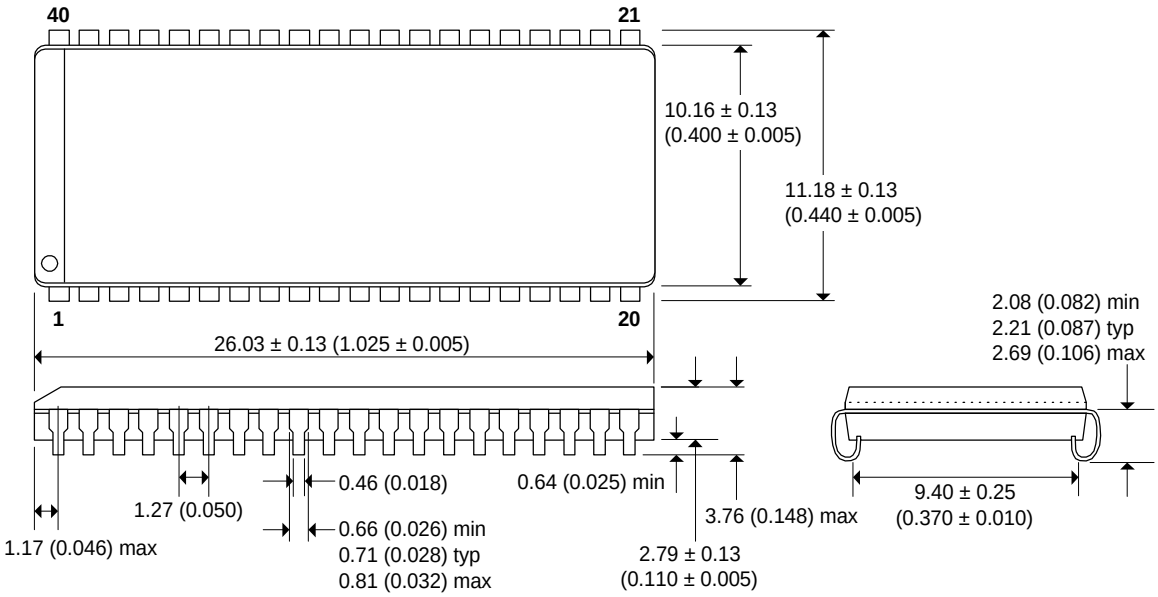
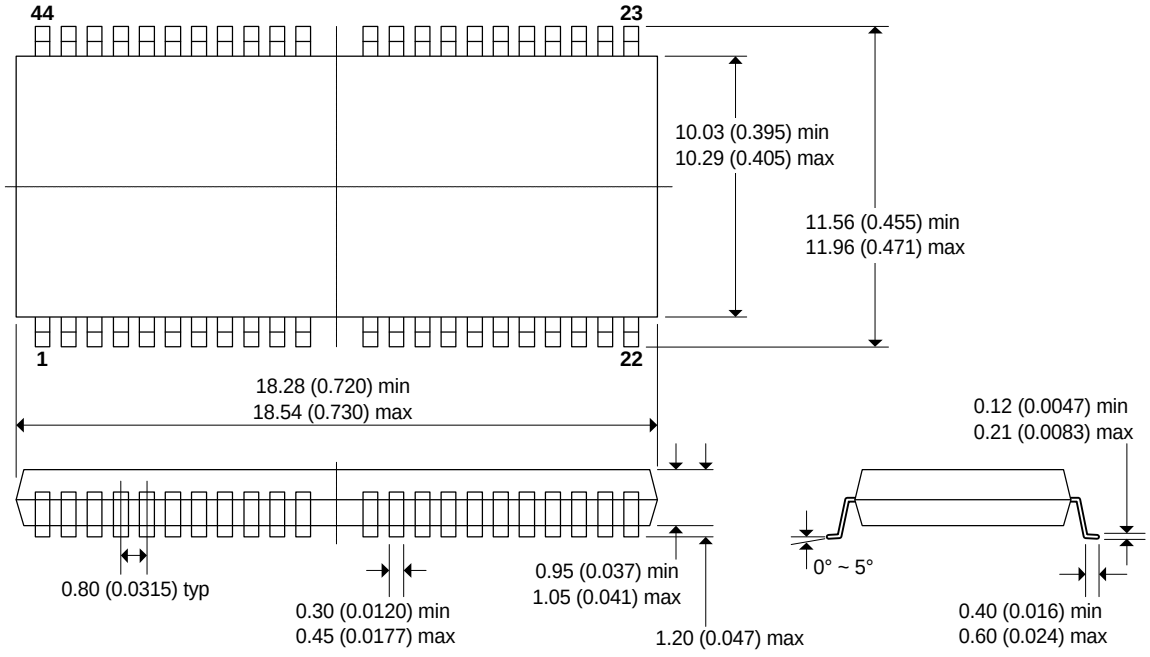
Package Information

40-Pin SOJ (400 mil)



44-pin TSOP II (400 mil)



Note: 1. All dimensions are given in millimeters (inches).
2. All dimensions are typical dimensions unless noted otherwise.

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