APPLICATION NOTE

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Frequency synthesis with the NE564

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FREQUENCY SYNTHESIS WITH THE NE564

Frequency multiplication can be achieved with the PLL in two ways:

a. Locking to a harmonic of the input signal

b. Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 1a. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications, it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is DC and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal), if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication, it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more under-damped loop transient response.

Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 1a. Large N values, in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (-M) is inserted as a prescaler as in Figure 1b to divide down the reference frequency input. This also gives more programming flexibility, since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_O' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 1b find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 27MHz range. Channel 4 uses 27.005MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals — one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency-mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example, one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

Since the function of frequency synthesizers is to generate frequencies and not to linearly decode or demodulate input signals, digital PLLs are more commonly used than analog loops.

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also, the phase comparator input and VCO output are compatible with TTL counters.
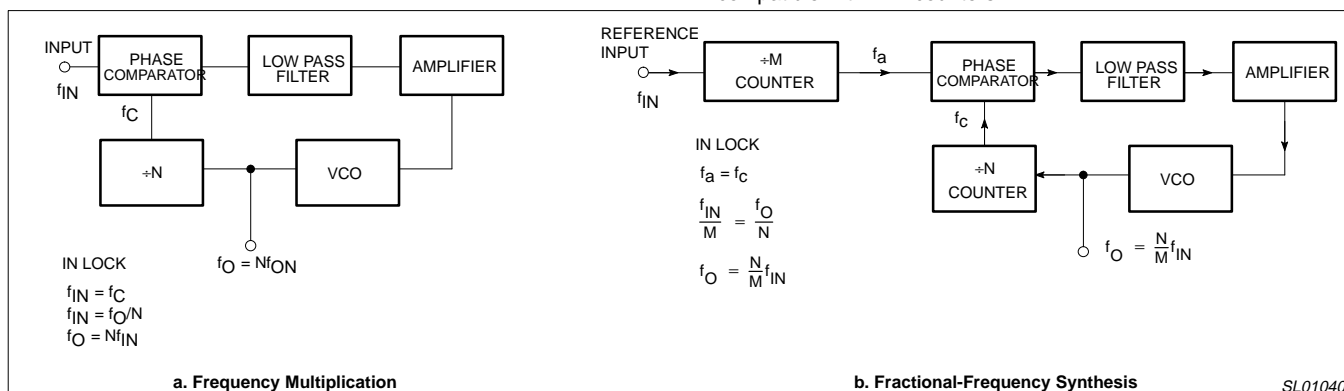

a. Frequency Multiplication

IN LOCK

$f_{IN} = f_C$

$f_{IN} = f_O/N$

$f_O = Nf_{IN}$

b. Fractional-Frequency Synthesis

IN LOCK

$f_a = f_c$

$\dfrac{f_{IN}}{M} = \dfrac{f_O}{N}$

$f_O = \dfrac{N}{M}f_{IN}$

$f_O = \dfrac{N}{M}f_{IN}$

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Figure 1. Frequency Synthesis Using PLLs

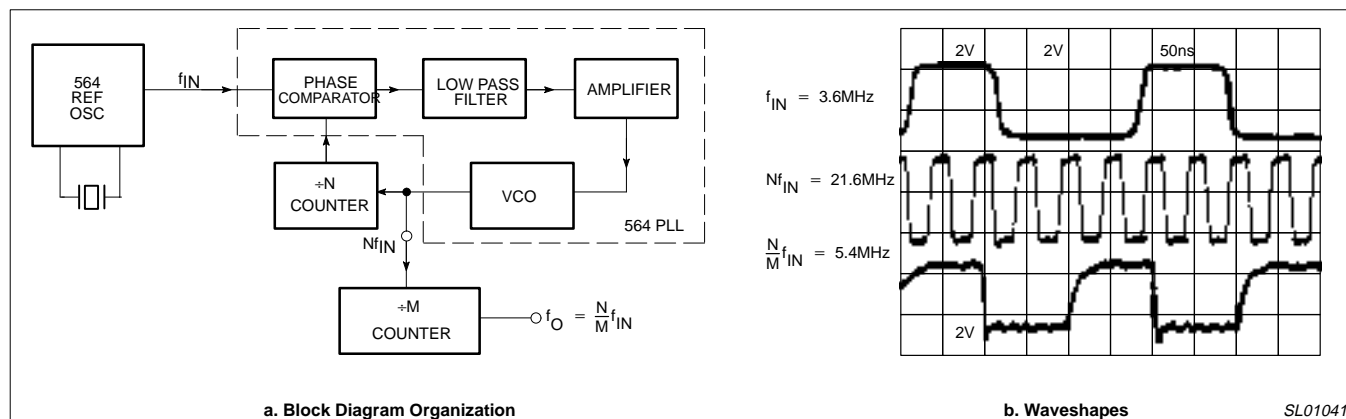# Frequency synthesis with the NE564

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Figure 2. Fractional Frequency Synthesis With the 564

NE564 FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 2 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequencydetermining element in the VCO of a second PLL. The thermal stability of all three frequencies will be the same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystal's resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_O' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally, counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparator's input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 2a where the +N counter becomes a +2N and M = 2 for the second counter.