Intel® StrongARM® SA-1101 Microprocessor Companion Chip

Specification Update

September 1999

Notice: The Intel® StrongARM® SA-1101 microprocessor companion chip may contain design defects or errors known as errata. Characterized errata that may cause the product to deviate from published specifications are documented in this specification update.

Order Number: 278231-007

Contents

Revision History

Date	Version	Description
09/07/99	007	Under Document Changes, transposed the the signal and BGA Pad for pin 20 in Table 21-2.
05/25/99	006	Under Document Changes, changed the value of the resistor connected to the IREF pin.
02/24/99	005	Under Document Changes, added change to Clock Divider Register; added change to RefCLK reference; added change to IEEE Config Register.
01/28/99	004	The documentation changes have been removed from the specification update and applied to the developer's manual. Under Affected Documents/Related Documents, removed SA-1101 Datasheet to show discontinuance; added registered trademark to the title.
01/15/99	003	Under Document Changes, changed buffer control signal in the PCCR.
11/03/98	002	Under Document Changes, added new Table 21-2.
10/19/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
StrongARM® SA-1101 Microprocessor Companion Chip Developer's Manual	278170-002
Intel® StrongARM® SA-1101 Microprocessor Companion Chip Brief Datasheet	278171-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	D	#	#			
1	X			11	NoFix.	Snooped Writes After Sleep May Fail
2	X			11	NoFix.	Bus Lock-Up on Entering Sleep
3	X			12	NoFix.	Set-Up Violation When Exiting From Sleep
4	X			12	Fix.	IrefEN and VCOON Are Not Reset on Entry to Sleep
5	X			12	NoFix.	Length of USB Port Reset Pulse Too Short on Power Up
6	X			12	Fix.	USB Pad Transistors Do Not Turn Off on Entry to Sleep

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278170-002	15	Doc	Clock Divider Register (SKCDR): Section 10.2.2
2	278170-002	15	Doc	RefClk references in Chapter 15
3	278170-002	15	Doc	IEEE Config Register: Section 11.3.1
4	278170-002	15	Doc	IREF Reference in Section 12.6.1
5	278170-002	15	Doc	Package and Power: Table 21-2

Identification Information

Markings

DE-S1101-AA.

Markings	Package
DE-S1101-AA	256 mBGA

This document contains errata for the StrongARM® SA-1101 Microprocessor Companion Chip (SA-1101). The SA-1101 device revision that is affected by this errata can be identified as order number DE-S1101-AA.

Errata

1. Snooped Writes After Sleep May Fail

Problem: This problem exists if BAT_FLT or VDD_FLT assert while there is new data in the Update FIFO (snooped but not yet written to the “dedicated” FB DRAM). This problem only exists in dedicated display memory mode of operation. Unified display memory mode of operation does not use the Update FIFO.

Implication: Several pixels, which were correctly snooped and written to the Update FIFO, might not be written correctly to the dedicated FB DRAM until the screen is redrawn.

Workaround: There are two workarounds.

1. Software can rewrite the pixels most recently snooped by the SA-1101 before the BAT_FLT or VDD_FLT condition is asserted. BAT_FLT or VDD_FLT assertion is a relatively rare and severe low-power event and should not impact performance.
2. Software-initiated sleep can disable snoop mode and empty the Update FIFO before shutting off BCLK and the Video Memory Controller (VMC). This ensures that all snooped pixels are flushed from the FIFO and written to the DRAM before going into the sleep condition. Update FIFO “fullness” and “empty” status flags in the Update FIFO Status Register (UFSR) can be read via register reads.

Status: NoFix.

2. Bus Lock-Up on Entering Sleep

Problem: This problem exists on entering the sleep condition via setting the sleep bit in the Control Register (SKCR) of the SA-1100 interface and Shared Memory Controller (SMC).

Implication: There is a narrow window of time in which a UsbReq or VidReq may assert and cause MBREQ to go high. The SA-1100 grants the bus to the SA-1101, but the SA-1101 has initiated the sleep sequence and does not do the expected USB or video cycle to shared memory, thus holding and locking up the SA-1100 bus.

Workaround: There are two workarounds.

1. For software-initiated sleep, set the sleep bit in the SKCR to disable the video and USB.
2. For BAT_FLT-induced sleep or VDD_FLT-induced sleep, assert BAT_FLT/VDD_FLT for more than 1 microsecond to allow the sleep state machine to shut off on-chip systems. While asserted they will prevent USB and video from requesting the SA-1100 bus. They should not be allowed to glitch.

Status: NoFix.

3. Set-Up Violation When Exiting From Sleep

Problem: A problem with the self-refresh logic exists when exiting from sleep on one of the Video Memory Controller (VMC) state machine bits (VMCstate[3] FF).

Implication: The Self-Refresh Request signal (SRReq) might change shortly before BCLK and violate set-up time. The sleep state machine is clocked by the external clock; the VMC is clocked by BCLK.

Workaround: To enter software-controlled sleep, set the Force Self-Refresh bit (VMCCR bit 31) before setting the sleep command bit. To exit software-controlled sleep, get out of the sleep condition and clear the Force Self-Refresh bit. Analysis of the VMC state machine indicates that, even if there was a metastability event, the VMC state machine will not enter “illegal” or unknown states. The VMC state machine will return unconditionally to “idle” state and then to “self-refresh” sequence as requested.

Status: NoFix.

4. IrefEN and VCOON Are Not Reset on Entry to Sleep

Problem: The phase-locked loop (PLL) is not shutting off when the SA-1101 enters sleep mode.

Implication: Only bit PLLEn (VCO Bypass) in the Control Register (SKCR) is cleared by the sleep state machine in its process of shutting down the SA-1101. The PLL continues operating and using power. The two bits that control power for the PLL (IrefEn and VCOON) are not reset on entry to sleep.

Workaround: External to the SA-1101, the IREF current can be supplied from a source that is switched on (asserted HIGH) for normal operation and off (LOW) for sleep mode. Cutting off the IREF current shuts down the PLL and reduces power. Any CMOS output in the system with the correct logical behavior will work because it is a low-current requirement. Care must be taken to filter IREF on the source side of the IREF resistor to prevent noise on the SA-1101 side.

Status: Fix.

5. Length of USB Port Reset Pulse Too Short on Power Up

Problem: The length of an USB Port Reset pulse is less than 10 microseconds although the specification requirement is >10 milliseconds. The reset pulse duration is generated by hardware counting out 1ms units of time from a timer, in response to setting the PRS bit in the RhPortStatus register of the USB Host Controller.

Implication: The nSimScaleDownClk bit in the USTCSR register substitutes a faster clock source for the 1ms clock. The SA-1101 powers up with this bit LOW, enabling the fast clock and causing the reset pulse to be too short.

Workaround: During the USB Host Controller reset sequence, set the nSimScaleDownClk bit in the USTCSR register HIGH before clearing the ForceHCReset bit.

Status: NoFix.

6. USB Pad Transistors Do Not Turn Off on Entry to Sleep

Problem: This problem exists when the SA-1101 enters the sleep mode. The measure IDD is approximately 180 µA (dependent on temperature), compared to a specification maximum of 20 µA.

Implication: Excess current in the current path in the USB pad driver.

Workaround: None.

Status: Fix.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. Clock Divider Register (SKCDR): Section 10.2.2

Divide by 0 changed to Divide by 1 for DivRValue and DivNValue.

2. RefClk references in Chapter 15

All references to RefClk in the PS/2 Trackpad and Mouse Interfaces Chapter (Chapter 15)

changed to PCLK.

3. IEEE Config Register: Section 11.3.1

The following table replaces the IEEE Config Register bit table:

Bit	Name	Function
2:0	M[2:0]	Mode select 1XX – Compatibility Mode 000 – Nibble Mode 001 – Byte Mode 010 – ECP Mode 011 – EPP Mode
3	D	FIFO access enable 0 – Register access 1 – FIFO access
4	B	9-bit word enable 0 – Disable 9 bit mode 1 – Enable 9 bit mode
5	R	Data transfer enable 0 – Transfer disabled 1 – Transfer enabled
6	T	Data transfer direction 0 – Peripheral-to-host (reverse) 1 – Host-to-peripheral
7	A	Timer enable 0 – Timer disabled 1 – Timer enabled
31:8	—	Reserved

4. IREF Reference in Section 12.6.1

The value of the resistor connected to the IREF pin has been changed to 26.7 K ohms. The text in this section now appears as follows:

The recommended connection of the IREF pin is with a 26.7 K resistor to VDD.

5. Package and Power: Table 21-2

Transpose the signal and BGA Pad for pin 20.

Table 21-2. SA-1101 Pinout — 256 Mini-Ball Grid Array

Pin	Signal	BGA Pad	Pin	Signal	BGA Pad	Pin	Signal	BGA Pad	Pin	Signal	BGA Pad
1	**VDD**	A11	65	**VDD**	F11	129	**VDD**	K6	193	**VDD**	L11
2	**VSS**	A1	66	**VSS**	G7	130	**VSS**	H9	194	**VSS**	K8
3	D31	B1	67	nRAS0	T1	131	PCM_ST0	T16	195	GPA3	A16
4	D29	C2	68	nCAS2	R2	132	S1_nIOIS16	P15	196	GPA6	B15
5	D30	C1	69	nCAS3	R3	133	VDD_FLT	R16	197	GPA5	B14
6	D28	D3	70	nRAS1	T2	134	S1_VCC0	P14	198	GPA2	A15
7	D27	D2	71	**VSS**	G8	135	PCM_ST1	P16	199	GPB3_KPY13	D13
8	D26	D1	72	nOE	T3	136	S1_nWAIT	N15	200	GPA1	A14
9	**VDD**	B5	73	nCAS0	P5	137	PCM_ST2	N16	201	GPA4	B13
10	**VSS**	B2	74	nCS	P4	138	S1_nWE	N14	202	GPA0	A13
11	D24	E3	75	nWE	R4	139	S1_VCC1	M14	203	GPB0_KPY10	C13
12	D23	E4	76	PSKTSEL	T4	140	**VDD**	K11	204	nFB_WE	C12
13	D25	E1	77	A19	N5	141	**VSS**	H10	205	nFB_LCAS	B12
14	D21	F4	78	nIOIS16	R5	142	PCM_ST3	M16	206	**VSS**	K10
15	D20	F3	79	nPOE	T5	143	S1_nIOWR	M13	207	**VDD**	M15
16	D19	F2	80	**VSS**	G9	144	S1_VPP0	L14	208	nFB_RAS	A12
17	D18	F1	81	**VDD**	F15	145	S1_nVS1	L12	209	FB_A0	D12
18	**VSS**	B8	82	nPIOR	P6	146	S1_nVS2	L13	210	FB_A5	C11
19	**VDD**	E2	83	PCM_ST6	T6	147	USB_MINUS	K13	211	FB_A6	B11
20	D22	F5	84	PCM_ST5	M6	148	USB_PLUS	K14	212	**VDD**	R6
21	D15	G3	85	nPWE	N6	149	S1_VPP1	L15	213	**VSS**	P3
22	D14	G4	86	nPCE1	P7	150	PCM_ST4	L16	214	FB_A1	D11
23	D13	G5	87	nPCE2	N7	151	**VSS**	J7	215	FB_A9	C10
24	D16	G2	88	nPWAIT	R7	152	**VDD**	L6	216	FB_A4	D10
25	D17	G1	89	S0_READY_nIREQ	T7	153	PWM2	K15	217	FB_A8	B10
26	D11	H4	90	nPIOW	M7	154	PWM1	K16	218	FB_A2	E11
27	D10	H3	91	S0_nCD2	N8	155	nTEST	K12	219	FB_A7	A10
28	D9	H1	92	S0_nCD1	P8	156	MSDATA	J14	220	FB_A3	E10
29	D12	H5	93	S0_nCE2	M8	157	TPCLK	J13	221	FB_D2	C9
30	**VSS**	C3	94	S0_nWE	R8	158	TPDATA	J12	222	FB_A10	D9
31	**VDD**	F7	95	S0_RESET	T8	159	MSCLK	J15	223	FB_A11	E9
32	D8	J1	96	**VDD**	G6	160	**VSS**	J8	224	FB_D3	B9
33	D7	J2	97	**VSS**	G10	161	**VDD**	L7	225	FB_D4	A9
34	**VSS**	C14	98	S0_nIOIS16	R9	162	PPDATA3_KPX3	H16	226	**VDD**	R12
35	D4	J5	99	S0_nCE1	M9	163	PPDATA4_KPX4	H15	227	**VSS**	R15
36	D5	J4	100	S0_nWAIT	P9	164	PPDATA7_KPX7	H12	228	FB_D5	A8
37	D6	J3	101	S0_nOE	N9	165	PPDATA5_KPX5	H14	229	FB_D0	E8
38	D3	K5	102	S0_BVD2_nSPKR	M10	166	PPDATA6_KPX6	H13	230	FB_D6	C8
39	nRESET	K1	103	S0_nVS1	T10	167	PPDATA2_KPX2	G16	231	FB_D1	D8
40	D0	K2	104	S0_nVS2	R10	168	PPDATA0_KPX0	G15	232	FB_D13	A7
41	D2	K4	105	S0_nIORD	N10	169	PPnINIT_KPY2	G12	233	FB_D12	B7
42	D1	K3	106	S0_nIOWR	P10	170	PPnSELECTIN_KPY1	G13	234	FB_D8	E7
43	**VDD**	F8	107	**VDD**	H6	171	PPnSTROBE_KPY0	G14	235	FB_D7	D7
44	**VSS**	D4	108	**VSS**	H2	172	PPDATA1_KPX1	F16	236	FB_D11	C7
45	MBGNT	L5	109	S0_BVD1_nSTSCHG	M11	173	**VSS**	J9	237	FB_D14	A6
46	INT	L2	110	S0_VPP0	T11	174	**VDD**	L8	238	PLL_VDD	B6
47	CLK	L3	111	S0_VPP1	R11	175	PPSELECT_KPY5	F12	239	**VDD**	G11
48	MBREQ	L4	112	S0_VCC0	P11	176	PPnAUTOFD_KPY3	F14	240	**VSS**	T9
49	A13	M4	113	S0_VCC1	N11	177	PPnACK_KPY4	F13	241	FB_D9	E6
50	A10	M1	114	S1_nCD1	N12	178	PPBUSY_KPY9	E13	242	PLL_VSS	C6
51	A11	M2	115	S1_BVD1_nSTSCHG	T12	179	PPPERROR_KPY6	E16	243	FB_D10	D6
52	A14	M5	116	**VSS**	H7	180	PPnFAULT_KPY7	E15	244	**VSS**	J16
53	A12	M3	117	**VDD**	H11	181	nFB_UCAS	E12	245	FB_D15	A5
54	A15	N1	118	S1_nCD2	P12	182	PPBUFEN_KPY8	E14	246	**VDD**	J6
55	A16	N2	119	S1_nOE	M12	183	BAT_FLT	D16	247	DAC_VDD	D5
56	**VSS**	E5	120	S1_nCE2	T13	184	**VSS**	J10	248	IREF	C5
57	**VDD**	F9	121	S1_nCE1	R13	185	**VDD**	L9	249	RED	A4
58	A17	N3	122	S1_READY_nIREQ	N13	186	GPB5_KPY15	D15	250	BLUE	B4
59	A20	P1	123	GPB6	P13	187	GPB4_KPY14	D14	251	GREEN	C4
60	A21	P2	124	S1_nIORD	T14	188	GPB2_KPY12	C16	252	VSYNC	A3
61	nCAS1	R1	125	S1_RESET	R14	189	GPB1_KPY11	C15	253	DAC_VSS	B3
62	A18	N4	126	S1_BVD2_nSPKR	T15	190	GPA7	B16	254	HSYNC	A2
63	**VSS**	F6	127	**VSS**	H8	191	**VSS**	K7	255	**VSS**	K9
64	**VDD**	F10	128	**VDD**	J11	192	**VDD**	L10	256	**VDD**	L1

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