Intel® StrongARM® SA-1100 Microprocessor

Specification Update

February 2000

Notice: The SA-1100 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1100's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278105-025

Contents

Revision History

Date	Version	Description
2/7/00	025	Under Documentation Changes, corrected wording in Table 2-1, updated Figure 10-4, updated Figure 10-5, clarified descriptions in Section 10.5.3, updated Figure 10-9 and modified parameters text in Section 10.4.4, and updated Figure 10-10, modified parameters text in Section 10.4.6, modified Section 9.5.2.2, and corrected register address assignments and register names in Appendix A. Under Specification Changes, added a product discontinuance notification.
12/21/99	024	Under Errata, added one errata documenting UDC work-around procedure.
12/20/99	023	Under Documentation Changes, modified Section 16.6.2.
11/19/99	022	Under Documentation Changes, revised Figure 2-2; changed package designations, changed table title, and added note to Table 12-3; added introductory sentence to and changed title of Table 13-2; added introductory sentence to Table 16-1.
11/05/99	021	Under Documentation Changes, added sentence to end of first paragraph in Section 9.5.2.2.
11/03/99	020	Under Documentation Changes, changed signal description of GPIO pin 25 in table in Section 9.1.2; added note to end of Section 11.11.6; deleted note to bit 3 of the RCSR register in Section 9.6.1.2; revised bit 0 description of UDCCR register in Section 11.8.3.8; replaced Section 11.10.2.3; corrected type in Table 9-3 title.
10/22/99	019	Under Documentation Changes, changed values for maximum sleep mode current and typical sleep mode current in Table 12-3; added paragraph at end of Section 8.2. Under Errata, added one errata.
10/8/99	018	Under Errata, added one errata.
09/15/99	017	Under Identification Information, converted all E stepping parts to G stepping parts. Under Documentation Changes, added footnote to the GPIO Alternate Functions Table in Section 9.1.2.
08/19/99	016	Under Documentation Changes, changed settings for serial port 4 in Table 11-6.
08/11/99	015	Documentation changes #2 - #18 have been removed from the specification update and applied to the technical reference manual; under Errata, added one errata.
07/22/99	014	Under Documentation Changes, changed code example for Section 6.2.3; changed last sentence of section 9.5.3; added output signals to Table 13-2.
06/21/99	013	Under Documentation Changes, removed section 16.8; changed Test Unit Control Register's description of bit 10; changed Section 9.5.7.7; changed section 9.5.6; changed section 11.13.1; changed section 11.13.6; removed the SA-1100 Tool Chains and Operating Systems Table from the brief datasheets and the developer's manual. Under Errata, changed SDLC errata status to NoFix for G stepping.
05/18/99	012	Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; corrected SA-1100 functional diagram. Under Markings, added G stepping markings.

Date	Version	Description
04/15/99	011	Documentation changes #2 - #10 have been removed from the specification update and applied to the technical reference manual; Rev G stepping information added; added doc change for big and little endian section 3.1; added documentation change for DRAM single-beat transactions Figure 10-3.
03/18/99	010	Under Documentation Changes, replaced Table 1-5; changed Section 9.5.2.1; removed section 11.12.9.3; changed current consumption units for the oscillator circuit.
02/24/99	009	Under Documentation Changes, added text change to Section 9.5.3.5; removed sentence from Section 10.6.2; changed wording in document change #1 from “all parameters guaranteed by design” to “all parameters verified by design”. Under Errata, added errata for possible PCMCIA second byte data corruption.
01/22/99	008	Under Documentation Changes, added architecture and implementation-defined identification for Register 0 of coprocessor 15; removed last sentence and changed text in the Note for Section 11.8.2; changed text in Section 10.3.2.
12/23/98	007	The document changes have been removed from the specification update and applied to the technical reference manual. The “Appendix D, Internal Test” specification change has been removed from the specification update and applied to the technical reference manual.
11/10/98	006	Under Specification Changes, added new Appendix D, Internal Test.
10/22/98	005	Under Affected Documents/Related Documents, added product discontinuance information. Under Specification Changes and Document Changes, added product discontinuance information. Under Markings, added product discontinuance information. Under Specification Changes, added product discontinuance information. Under Document Changes, added change to Table 1-1, Table 1-2, Table 8-1, and Section 11.12.4.1. Under Errata, added errata for slow SIR.
09/25/98	004	Under Affected Documents/Related Documents, added StrongARM to precede SA-1100 in the titles for the two brief datasheets.
09/18/98	003	Under Identification Information, removed DE-S1100-BA and DE-S1100-BB to show discontinuance. Under Documentation Changes, removed references to -BA and -BB parts to show discontinuance. On the title page, StrongARM added to precede SA-1100 in the title.
08/25/98	002	Under Documentation Changes, changed page, table, and figure #s to show change to Intel format. Added change to Table 12-1, Table 12-2, Table 12-3, Table 13-1, Table 13-2, Figure 14-1 and Section 3.2.6. Under Identification Information, added DE-S1100-EA, DE-S1100-AB, DE-S1100-BB, DE-S1100-CB, DE-S1100-DB, AND DE-S1100-EB. Under Affected Documents/Related Documents, removed SA-1100 Data Sheet to show discontinuance. Under Errata, added two errata.
07/14/98	001	Product line order number sequence change, from 280105-001 to 278105-001. Under Affected Documents/Related Documents, changed order #s to show change to Intel order #s.
06/15/98	001	This is the new specification update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM® SA-1100 Microprocessor Technical Reference Manual	278088-004
Intel® StrongARM® SA-1100 Microprocessor for Portable Applications Brief Datasheet	278087-006

08/25/98
Removed reference to the StrongARM™ SA-1100 Microprocessor Datasheet (278179-001) as it is no longer in publication.

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1100 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	E	G	#			
1	X	X		14	No Fix.	Possible Missed RTC Alarm
2	X	X		14	No Fix.	Transmit Behavior Causing Generation of Five Consecutive Ones at End of CRC
3	X	X		14	No Fix.	Restriction on Clearing LCD AC Bias Count (ABC) Status Bit
4	X			15	Fix.	Receiver to Receive Data Frequency in Slow Infrared Mode (SIR)
5	X			15	Fix.	Incorrect Transmit Pulse Width in Low-Power Mode in Slow Infrared Mode (SIR)
6	X			15	Fix.	Possible Corrupted Start Bit in Slow Infrared Mode (SIR)
7	X	X		15	No Fix.	Possible PCMCIA Second Byte Data Corruption
8	X	X		16	No Fix.	USB Must Be in a Single Client Environment
9	X	X		16	No Fix.	Incorrect Sign-Extended Value in Register After a Read Buffer Allocate
10	X	X		16	No Fix.	DRAM Refresh Corrupting ROM Burst of 4/8 Timing
11.	X	X	X	16	Eval.	UDC Not Responding to IN Packet After Receiving an SOF Packet

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	E	G			
1	X		17	Eval	USB Feature
2	X		17	Doc	Product Discontinuance
3	x		17	Doc	Product Discontinuance -- GDDES1100xG

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278088-004	19	Doc	AC Timing Table: Table 13-2
2	278088-004	19	Doc	Valid Settings for the DDARn Register: Table 11-6
3	278087-006	19	Doc	SA-1100 Characteristics: Table 2
4	278088-004	20	Doc	GPIO Alternate Functions Table: Section 9.1.2
5	278088-004	20	Doc	SA-1100 Power Supply Voltages and Currents with TQFP Package: Table 12-3
6	278088-004	20	Doc	Core Clock Configuration Register: Section 8.2
7	278088-004	21	Doc	GPIO Alternate Functions: Section 9.1.2
8	278088-004	21	Doc	UART Data Register: Section 11.11.6
9	278088-004	21	Doc	Reset Controller Status Register: Section 9.6.1.2
10	278088-004	21	Doc	Reset Interrupt Mask: Section 11.8.3.8
11	278088-004	21	Doc	Address Field: Section 11.10.2.3
12	278088-004	21	Doc	Pin State During Sleep: Table 9-3
13	278088-004	21	Doc	Exiting Idle Mode: Section 9.5.2.2
14	278088-004	22	Doc	SA-1100 Functional Diagram: Figure 2-2
15	278088-004	23	Doc	SA-1100 Power Supply Voltages and Currents: Table 12-3
16	278088-004	23	Doc	SA-1100 AC Timing Table: Table 13-2
17	278088-004	23	Doc	SA-1100 Boundary-Scan Timing Interface Timing: Table 16-1
18	278088-004	24	Doc	SA-1100 Device Identification (ID) Code Register: Section 16.6.2
19	278088-004	24	Doc	Signal Description: Section 2.3
20	278088-004	25	Doc	DRAM Timing: Section 10.3.2
21	278088-004	26	Doc	DRAM Refresh: Section 10.3.3
22	278088-004	26	Doc	DRAM Access Followed by a Refresh Operation: Section 10.5.3
23	278088-004	27	Doc	SRAM Timing Diagrams and Parameters: Section 10.4.4
24	278088-004	28	Doc	FLASH EPROM Timing Diagrams and Parameters: Section 10.4.6
25	278088-004	28	Doc	Exiting Idle Mode: Section 9.5.2.2
26	278088-004	29	Doc	Register Summary: Appendix A

Identification Information

Ordering Information

This document contains errata for the SA-1100 Microprocessor. The SA-1100 device revision that is affected by this errata can be identified by the following ordering numbers:

E Stepping Ordering Numbers	Speed (MHz)	Voltage (V)	Package
DE-S1100-AA	133	1.5	TQFP
DE-S1100-CA	160	2.0	TQFP
DE-S1100-DA	220	2.0	TQFP
DE-S1100-EA	190	1.5	TQFP
DE-S1100-AB	133	1.5	mBGA
DE-S1100-CB	160	2.0	mBGA
DE-S1100-DB	220	2.0	mBGA
DE-S1100-EB	190	1.5	mBGA

09/16/98
Removed ordering numbers DE-S1100-BA and DE-S1100-BB to show product discontinuance.

G Stepping Ordering Numbers	Speed (MHz)	Voltage (V)	Package
FADES1100AF	133	1.5	TQFP
FADES1100CF	160	2.0	TQFP
FADES1100DF	220	2.0	TQFP
FADES1100EF	190	1.5	TQFP
GDDES1100AG	133	1.5	mBGA
GDDES1100CG	160	2.0	mBGA
GDDES1100DG	220	2.0	mBGA
GDDES1100EG	190	1.5	mBGA

07/99
The following G step ordering numbers are active: FADES1100EF and GDDES1100EG.
The following E step ordering numbers are inactive: DE-S1100-EA and DE-S1100-EB.

09/99
The following G step ordering numbers are active: FADES1100AF, FADES1100CF, FADES1100DF, GDDES1100AG, GDDES1100CG, and GDDES1100DG.
All E step ordering numbers are inactive.

Related Information

None for this revision of this specification update.

Errata

1. Possible Missed RTC Alarm

Problem: If an RTC alarm occurs just as the SA-1100 is entering or leaving sleep mode, the alarm status bit (AL, bit 0 in RTSR) could fail to be set.

Workaround: A software workaround intended to provide a way to avoid missing an RTC alarm is available. If the RTC alarm is set:

1. Read the RTC Timer (RCNR) and Alarm register (RTAR) before entering sleep mode via software. The RTAR must be greater than or equal to RCNR + 2 in order to ensure that an RTC alarm is not missed while entering sleep mode.
2. Read the RTC Timer (RCNR) and Alarm register (RTAR) after a sleep wakeup to determine if an alarm occurred.

Status: No Fix.

2. Transmit Behavior Causing Generation of Five Consecutive Ones at End of CRC

Problem: If the data within a packet transmitted by the SDLC transmitter causes the last five bits within the CRC to be all ones, the SDLC does not insert a zero into the serial data being output.

For example, the SDLC transmits the following:

start | addr | cntl | data | CRC...011111 | 01111110 |

when it should transmit:

start | addr | cntl | data | CRC...0111110 | 01111110 |

The SDLC receiver does not strip a zero after five ones are encountered at the end of the receive packet CRC. However, the SDLC receiver correctly detects a packet either with or without a stuffed zero at the end.

Workaround: None. Off-chip receivers can signal errors when detecting data that causes five consecutive ones to be generated at the end of the CRC.

Status: No Fix.

3. Restriction on Clearing LCD AC Bias Count (ABC) Status Bit

Problem: If the user programs the AC Bias Pin Transition Per Interrupt (API) bit-field to a nonzero value and the AC Bias Count (ABC) status bit is set, writing a one to the bit does not clear it. Only a reset of the SA-1100 can clear the ABC.

Workaround: The API should be programmed to all zeros.

Status: No Fix.

4. Receiver to Receive Data Frequency in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode and the remote transmitter frequency is higher by 0.13 % or more than the SP2 Sir receiver clock supplied by the 3.6864-MHz PLL and bit rate generator, some percentage of the received data is corrupted by the addition of spurious bit.

Note: According to *IrDA Serial Infrared Physical Layer Link Specification V 1.2*, the allowable rate deviation tolerance is ± 0.87% when operating in SIR mode.

Workaround: None. Off-chip IrDA receivers can be used to format and synchronize the incoming data so that it can be input to the on-chip UART via SP2.

Status: Fix.

5. Incorrect Transmit Pulse Width in Low-Power Mode in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode and the UART control register 4 (UTCR4) LPB bit is set, the transmitted pulse is equal to 3/8 of a bit time.

Note: According to *IrDA Serial Infrared Physical Layer Link Specification V 1.2*, the nominal minimum pulse width is 1.63 µs regardless of the signaling rate when operating in low-power SIR mode.

Workaround: Do not use low-power (LPM) mode in SIR. Always set LPM of UTCR4 to zero.

Status: Fix.

6. Possible Corrupted Start Bit in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode, there is the possibility that the loading of the Transmit FIFO while the IrDA transmitter is active can cause the transmitted start bit to be corrupted. If the problem occurs, the start bit will go active 5/16 of a bit-time too early and will remain active for 8/16 of a bit-time, instead of the required time of 3/16 of a bit-time.

Workaround: None. Off-chip IrDA transmitters can be used to format the outgoing data from the on-chip UART via SP2.

Status: Fix.

7. Possible PCMCIA Second Byte Data Corruption

Problem: On a 16-bit data write to PCMCIA I/O space, bits [15:8] may be corrupted if the device does not assert nIOIS16, which forces two back-to-back 8-bit writes to the device. This can happen if any read/write transfers to/from addresses other than those served by the Memory and PCMCIA Control Module (that is, the Peripheral Module, the System Control Module, the LCD and DMA registers) during the PCMCIA write operation.

Implication: Unless the user controls the source code of the PCMCIA drivers allowing for a 16-bit data write to be broken into two 8-bit writes, 8-bit PCMCIA cards should not be used.

Workaround: If using an 8-bit PCMCIA device, allow only 8-bit write operations to the PCMCIA port.

Status: No Fix.

8. USB Must Be in a Single Client Environment

Problem: The client USB function on the SA-1100 stalls when more than one USB client is present in the USB system. The stall occurs after the host USB has finished a transmission to another client and the SA-1100 USB does not recognize this transmission as being completed. The SA-1100 USB then ignores any transmission addressed to the SA-1100.

Workaround: Allow only one client USB in the system.

Status: No Fix.

9. Incorrect Sign-Extended Value in Register After a Read Buffer Allocate

Problem: After a read buffer allocate, a Load Register Signed Halfword (LDRSH) or a Load Register Signed Byte (LDRSB) will not return the correct value in the register, due to long propagation delays in the sign extend logic.

Workaround: Execute the command twice and the data is guaranteed to be correctly sign extended for the second read.

Status: No Fix.

10. DRAM Refresh Corrupting ROM Burst of 4/8 Timing

Problem: Asynchronous DRAM refreshes are allowed to interrupt burst transfers to any static, asynchronous memory type (ROM or SRAM) between 32-bit transfers. This works properly when any of those memory types are configured for non-burst timings (MSCx:RTx = 0 or 1). But, when ROM is configured for burst timings (MSCx:RTx = 2 or 3), burst-of-4/8 aligned addresses may erroneously use the burst access time (MSCx:RDNx) rather than the intended non-burst access time (MSCx:RDFx). This happens whenever the refresh request (internally generated) occurs just prior to a burst-of-4/8 unaligned address. The problem will affect burst-of-4 timings on either 16-bit or 32-bit data busses, or burst-of-8 timings on 16-bit data busses.

Workaround: Use non-burst timing (MSCx:RTx = 0) for ROM.

Status: No Fix.

11. UDC Not Responding to IN Packet After Receiving an SOF Packet

Problem: The host will request data from the UDC by sending an IN packet to Endpoint 2. The UDC must respond with a NAK signal if it does not currently have any data stored in the FIFO. Sporadically, the UDC will not respond with a NAK signal after an SOF packet has been received.

Workaround: Connect a USB hub between the UDC and the host system.

Status: Eval.

Specification Changes

1. USB Feature

The USB feature is available effective with the Rev G stepping.

2. Product Discontinuance

Effective October 16, 1998, Intel will no longer offer a 200 MHz version of the SA-1100 RISC microprocessor due to a product line consolidation. It is replaced by a new version of the same device offered at 190 MHz @ 1.5 V. This device can be ordered in both a TQFP and mBGA package.

3. Product Discontinuance -- GDDES1100xG

The SA-1100 product in the miniBGA package, base saleable part number GDDES1100xG, has been discontinued. The SA-1100 Microprocessor (mBGA) part numbers that have been discontinued are:

- GDDES1100AG — 133 MHz
- GDDES1100CG — 160 MHz
- GDDES1100EG — 190 MHz
- GDDES1100DG — 220 MHz

Last Product Order Date (firm, non–cancelable orders): 30 Jun 2000
Last Ship Date: 29 Sep 2000

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. AC Timing Table: Table 13-2

All parameters verified by design. Data needs to be added for CA and DA parts.

2. Valid Settings for the DDARn Register: Table 11-6

Settings for serial port 4 in Table 11-6 changed to:

Unit Name	Function	Device Address	DDAR Fields					
			DA<31:8>	DS<3:0>	DW	BS	E	RW
Serial port 0	UDC transmit	0x 8000 0028	0x80000A	0000	0	1	0/1	0
	UDC receive	0x 8000 0028	0x80000A	0001	0	1	0/1	1
Serial port 1	SDLC transmit	0x 8002 0078	0x80801E	0010	0	0	0/1	0
	SDLC receive	0x 8002 0078	0x80801E	0011	0	0	0/1	1
	UART transmit	0x 8001 0014	0x804005	0100	0	0	0/1	0
	UART receive	0x 8001 0014	0x804005	0101	0	0	0/1	1
Serial port 2	HSSP transmit	0x 8004 006C	0x81001B	0110	0	1	0/1	0
	HSSP receive	0x 8004 006C	0x81001B	0111	0	1	0/1	1
	UART transmit	0x 8003 0014	0x80C005	0110	0	0	0/1	0
	UART receive	0x 8003 0014	0x80C005	0111	0	0	0/1	1
Serial port 3	UART transmit	0x 8005 0014	0x814005	1000	0	0	0/1	0
	UART receive	0x 8005 0014	0x814005	1001	0	0	0/1	1
Serial port 4	MCP transmit (audio)	0x 8006 0008	0x818002	1010	1	1	0/1	0
	MCP receive (audio)	0x 8006 0008	0x818002	1010	1	1	0/1	1
	MCP transmit (telecom)	0x 8006 000C	0x818003	1100	1	1	0/1	0
	MCP receive (telecom)	0x 8006 000C	0x818003	1101	1	1	0/1	1
	SSP transmit	0x 8007 006C	0x81C01B	1110	1	1	0/1	0
	SSP receive	0x 8007 006C	0x81C01B	1111	1	1	0/1	1

3. SA-1100 Characteristics: Table 2

Removed part numbers from Table 2 to show that all E stepping parts were converted to G stepping parts. See Section , “Identification Information” on page 12 for more information.

4. GPIO Alternate Functions Table: Section 9.1.2

Added the following footnote to the GPIO Alternate Functions Table in Section 9.1.2:

†To enable RCLK_OUT, it is also necessary to set bits 31:29 of the Test Unit Control Register (TUCR) = 0b100. See Appendix D for more information about the TUCR.

5. SA-1100 Power Supply Voltages and Currents with TQFP Package: Table 12-3

The following values changed for maximum sleep mode current and typical sleep mode current:

Table 12-3. SA-1100 Power Supply Voltages and Currents with TQFP Package

Parameter	SA-1100				Units
	AA/AB†	CA/CB†	DA/DB†	EA/EB†	
Maximum operating frequency	133	160	220	190	MHz
Maximum run mode power (total VDD + VDDX)	400	1100	1100	500	mW
Typical run mode power (total VDD + VDDX)	230	430	550	330	mW
Maximum idle mode power†† (total VDD + VDDX)	55	n/a	n/a	85	mW
Typical idle mode power†† (total VDD + VDDX)	50	n/a	n/a	65	mW
Maximum sleep mode current †† (total VDD + VDDX, with VDD = 0)	50	n/a	n/a	50	uA
Typical sleep mode current †† (total VDD + VDDX, with VDD = 0)	25	n/a	n/a	30	uA
VDD					
Minimum internal power supply voltage	1.42	1.90	1.90	1.42	V
Nominal internal power supply voltage	1.50	2.00	2.00	1.50	V
Maximum internal power supply voltage	1.58	2.10	2.10	1.58	V
VDDX					
Minimum external power supply voltage	3.00	3.00	3.00	3.00	V
Nominal external power supply voltage	3.30	3.30	3.30	3.30	V
Maximum external power supply voltage	3.60	3.60	3.60	3.60	V

6. Core Clock Configuration Register: Section 8.2

The following paragraph added to Section 8.2:

The actual core clock (DCLK) can switch between being driven by the high speed core clock (CCLK, set by CCF< 4:0>) and the memory clock (MCLK), which runs at half the frequency of CCLK. CCLK is used except when the SA-1100 is waiting for fills to complete after a cache miss. At reset, clock switching is disabled and the DCLK is driven by MCLK. Clock switching can also be disabled by writing to CP15 register 15 with OPC_2 = 2 and CRm = 2 (see Section 5.2.14). Clock switching is enabled by writing to CP15 register 15 with OPC_2 = 2 and CRm = 1. Disabling clock switching only disables switching for DCLK; it does not force the DCLK to MCLK. However, DCLK can be forced to MCLK by forcing an instruction or data cache miss after clock switching is disabled.

7. GPIO Alternate Functions: Section 9.1.2

In the table showing each GPIO pin and its corresponding alternate function, changed the signal description for GPIO pin 25 from “Trimmed 1-Hz clock” to “Real time clock”.

8. UART Data Register: Section 11.11.6

Added the following note to the end of section 11.11.6:

Note: There may be a delay between the writing of data in the transit FIFO and the assertion of TBY in UTSR1. When the TBY status bit is set, there is some propagation delay for data moving through the FIFO and getting to the serial shifter. The programmer should either use the interrupt functionality of the UART module or wait for a 0 to 1 transition and then a 1 to 0 transition of TBY to ensure that the data is transmitted.

9. Reset Controller Status Register: Section 9.6.1.2

Deleted “Note” to description of RCSR register bit 3.

10. Reset Interrupt Mask: Section 11.8.3.8

Revised description of UDCCR register bit 0 as follows:

Bit	Name	Description
0	UDD	UDD disable. 0 – UDD enabled, UDC+ and UDC- used for USB serial transmission/reception. 1 – UDD disabled.

11. Address Field: Section 11.10.2.3

Section 11.10.2.3. replaced with the following text:

“The 8-bit address field is used by a transmitter to target a select group of receivers when multiple stations are connected to the same set of serial lines. The address allows up to 255 stations to be uniquely addressed (00000000 to 11111110). The global address (11111111) is used to broadcast messages to all stations. Register HSCR1 is used to program a unique address for broadcast recognition. Control bit HSCR0:AME is used to enable/disable the address match function. Note that the address of received frames is stored in the receive FIFO along with normal data and that it is transmitted and received starting with its LSB and ending with its MSB.”

12. Pin State During Sleep: Table 9-3

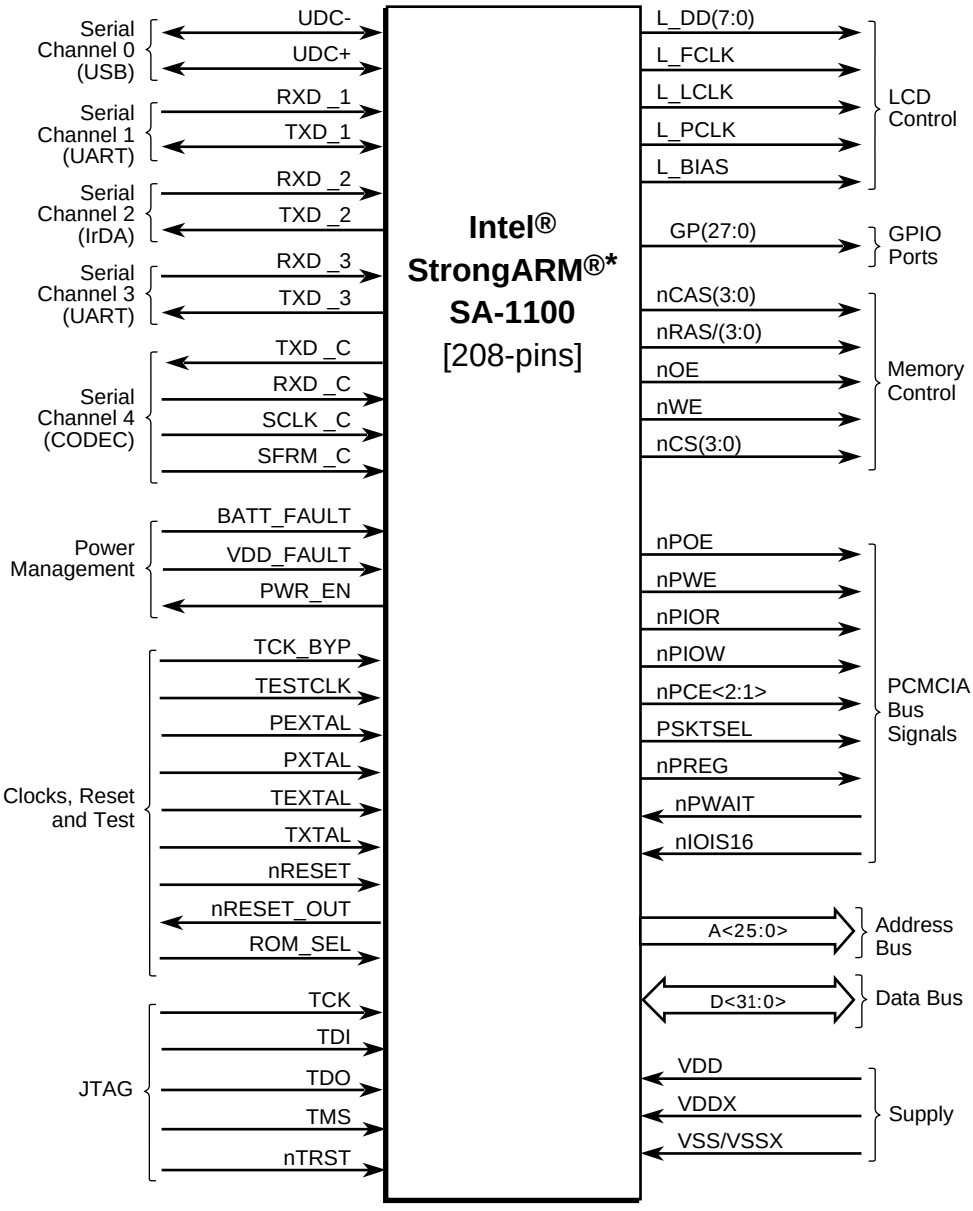
Corrected typo in title from “Pin State During Step” to “Pin State During Sleep”.

13. Exiting Idle Mode: Section 9.5.2.2

Added the following sentence to the end of first paragraph: “Note that the user should re-enable clock switching.”

14. SA-1100 Functional Diagram: Figure 2-2

Changed label for Serial Channel 1.



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15. SA-1100 Power Supply Voltages and Currents: Table 12-3

Changed title of table, changed package designations to Rev G stepping designations, and added a "Note" to the table as shown:

Table 12-3. SA-1100 Power Supply Voltages and Currents

Parameter	SA-1100				Units
	AF/AG†	CF/CG†	DF/DG†	EF/EG†	
Maximum operating frequency	133	160	220	190	MHz
Maximum run mode power (total VDD + VDDX)	400	1100	1100	500	mW
Typical run mode power (total VDD + VDDX)	230	430	550	330	mW
Maximum idle mode power†† (total VDD + VDDX)	55	n/a	n/a	85	mW
Typical idle mode power†† (total VDD + VDDX)	50	n/a	n/a	65	mW
Maximum sleep mode current †† (total VDD + VDDX, with VDD = 0)	50	n/a	n/a	50	uA
Typical sleep mode current †† (total VDD + VDDX, with VDD = 0)	25	n/a	n/a	30	uA
VDD					
Minimum internal power supply voltage	1.42	1.90	1.90	1.42	V
Nominal internal power supply voltage	1.50	2.00	2.00	1.50	V
Maximum internal power supply voltage	1.58	2.10	2.10	1.58	V
VDDX					
Minimum external power supply voltage	3.00	3.00	3.00	3.00	V
Nominal external power supply voltage	3.30	3.30	3.30	3.30	V
Maximum external power supply voltage	3.60	3.60	3.60	3.60	V

† AF, CF, DF and EF refer to TQFP package. AG, CG, DG and EG refer to mBGA package.

†† Room temperature specification.

Only maximum values are guaranteed by manufacturing test screen.

16. SA-1100 AC Timing Table: Table 13-2

Changed title of table and added the following introductory sentences:

"Table 13-2 lists the ac timing parameters for 133- and 190-MHz devices. These parameters are design guidelines only and are not guaranteed by manufacturing test screen."

17. SA-1100 Boundary-Scan Timing Interface Timing: Table 16-1

Added the following introductory sentence to Table 16-1:

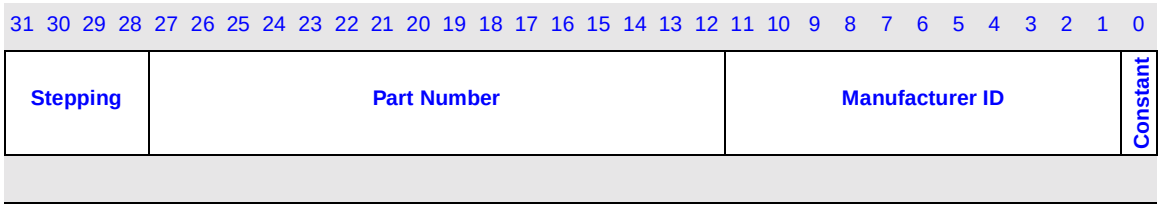
"These specifications are design guidelines only and are not guaranteed by manufacturing test screen."

18. SA-1100 Device Identification (ID) Code Register: Section 16.6.2

Section modified as follows:

This register is used to read the 32-bit device identification code. No programmable supplementary identification code is provided. When the IDCODE instruction is current, this register is selected as the serial path between TDI and TDO. The 32-bit device identification code is loaded into the register from its parallel inputs during the CAPTURE-DR state.

SA-1100 Device Identification (ID) Code Register — **Read-Only**



Stepping	Stepping revision of the SA-1100 0001 = B stepping 0010 = C stepping 0100 = D stepping 1001 = E stepping 1010 = F stepping 1011 = G stepping
Part Number	Part number 0001000010000100 = SA1100
Manufacturer ID	Manufacturer ID 00000110101 = Digital Semiconductor
Constant	1

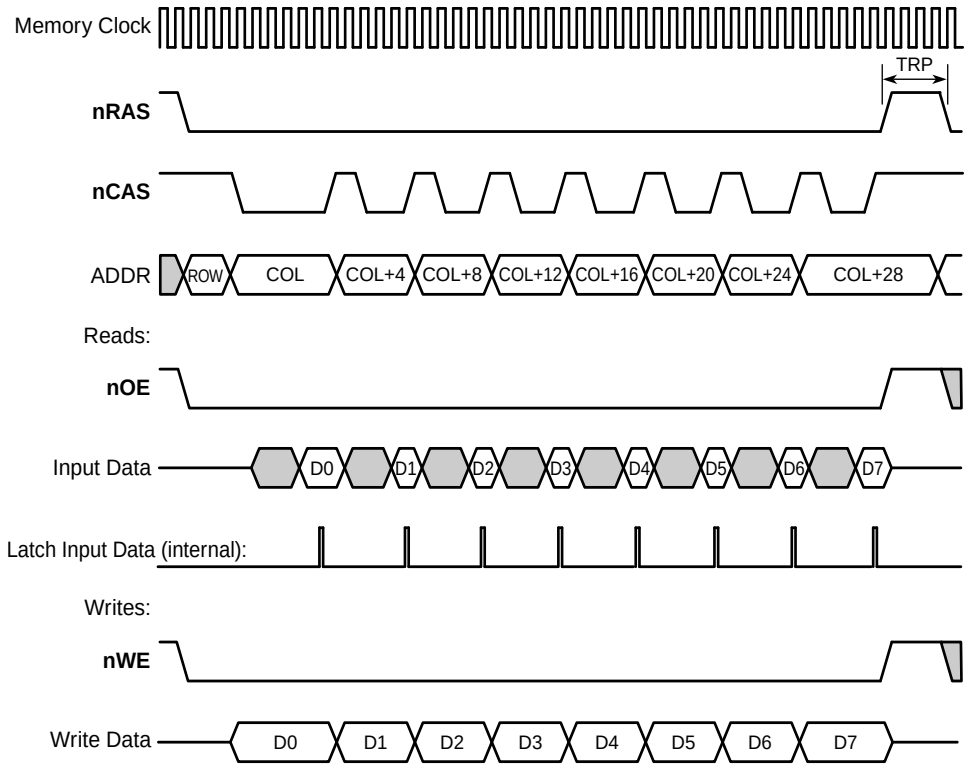
19. Signal Description: Section 2.3

The description column for Table 2-1, in the VDD_Fault row, is as follows:

"VDD fault. This signals the SA-1100 that the main power supply is going out of regulation (shorted card is inserted) prompting the SA-1100 to enter sleep mode. VDD_FAULT is ignored following a wake-up event until the power supply timer completes its current cycle (approximately 10 ms)."

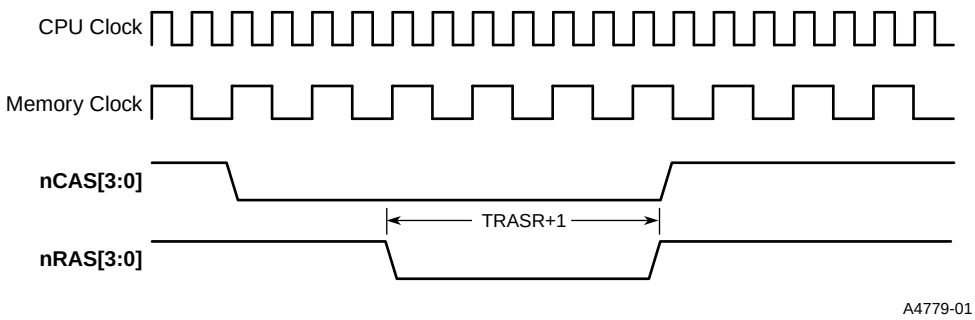
20. DRAM Timing: Section 10.3.2

Update Figure 10-4 as shown below.



21. DRAM Refresh: Section 10.3.3

Update Figure 10-5 as shown below.



22. DRAM Access Followed by a Refresh Operation: Section 10.5.3

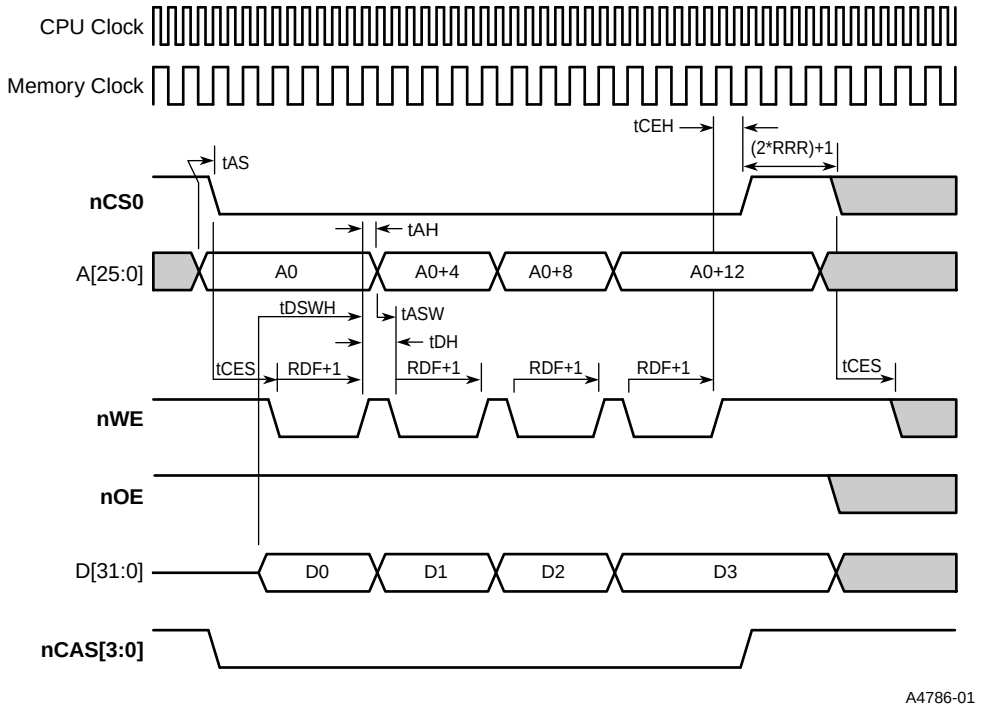
This section is changed as follows:

"At the end of a DRAM read/write cycle, nCAS will go high 1/2 to 1 memory clock cycles before nRAS goes high. For a subsequent refresh cycle, nCAS stays high for TRP+1 memory clock cycles after nRAS goes high. Following this, nCAS goes low while nRAS remains high for two successive memory clock cycles. In this case, TRP holds off nCAS and nRAS.

Note: There is no pipelining between successive memory accesses."

23. SRAM Timing Diagrams and Parameters: Section 10.4.4

Update Figure 10-9 as shown below.

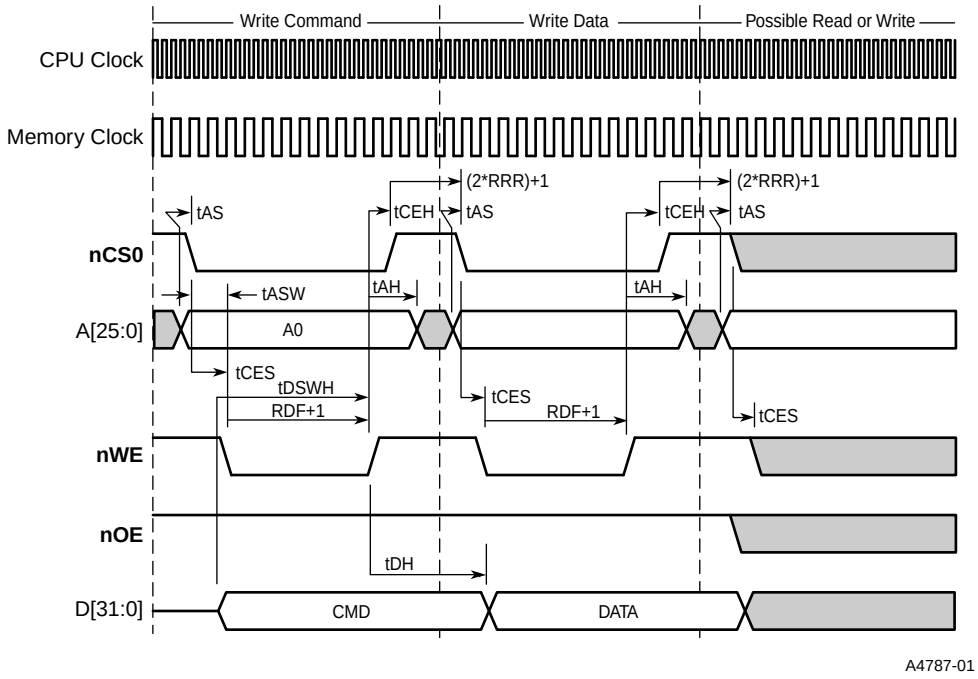


Changed the “tDSWH = Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDN+1) memory cycles” line in the parameters list (following the figure) to:

“:tDSWH = Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDF+1) memory cycles”

24. FLASH EPROM Timing Diagrams and Parameters: Section 10.4.6

Update Figure 10-10 as shown below.



Changed the “tDSWH = Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDN+1) memory cycles” line in the parameters list (following the figure) to:

“tDSWH = Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDF+1) memory cycles”

25. Exiting Idle Mode: Section 9.5.2.2

This section is must change as follows:

“Any enabled interrupt from the system unit or peripheral unit causes a transition from idle mode back to run mode. An interrupt does not need to be unmasked to bring the SA-1100 out of idle mode.Therefore, the Interrupt Controller Mask Register (ICMR) is ignored during idle mode. When an interrupt occurs, the CPU clocks are reactivated, the wait-for-interrupt instruction is completed, and run-program flow resumes. If the interrupt bringing the SA-1100 out of idle mode is masked, program flow resumes in a linear fashion. If the interrupt bringing the SA-1100 out of idle mode is unmasked, program flow resumes in any other interrupt service routine. Reenable clock switching for both circumstances.

A transition from idle to run mode can also occur by asserting the nRESET pin or if OSMR<3> is configured as a watchdog and a match occurs that causes the assertion of reset. Since the watchdog timer (if enabled) is functional during idle, care must be taken to set the watchdog match register far enough in advance to ensure that another interrupt is guaranteed to bring the SA-1100 out of idle before the watchdog reset occurs. Either an RTC alarm or another OS timer channel must be used for this purpose.

When in idle mode, if the BATT_FAULT or VDD_FAULT pins are asserted, the SA-1100 enters sleep mode.”

26. Register Summary: Appendix A

In the UART Registers (Serial Port 2) section of this table, change the UTCR2 entry to read as follows:

- Physical Address: 0h 8003 0008
- Symbol: UTCR2
- Register Name: UART control register 2

In the Interrupt Controller Registers section of this table, change the ICPR entry to read as follows:

- Physical Address: 0h 9005 000C
- Symbol: ICCR
- Register Name: Interrupt controller control register.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