# Intel® StrongARM® SA-110/21285 Evaluation Board

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## Product Overview

The Intel® StrongARM® SA-110/21285 Evaluation Board (EBSA-285) provides a flexible hardware development environment for the quick time-to-market design of applications based on the SA-110 microprocessor and 21285 core logic chip.

The EBSA-285 is the optimal solution for designing software and hardware prototypes, porting operating systems and applications, verifying hardware design, running ARM® V4 architecture-compliant software test suites and software benchmarks and building PCI-based systems that incorporate one or more SA-110 microprocessors.

The evaluation board can help shrink the development cycle by enabling software testing prior to the availability of hardware systems. For software developers, the platform simplifies code generation and benchmarking, simulation of processors and memory, and fast and efficient debugging.

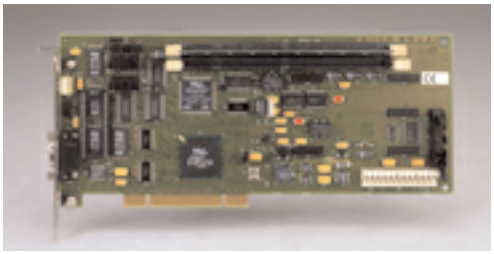
The EBSA-285 contains processor, system controller, memory, input/output devices, and a passive backplane (EBSA-BPL). The hardware developer's kit is complete with detailed, royalty-free application examples. The board is also available as a subset of the SA-110/21285 Hardware Developer's Kit.

## Product Highlights

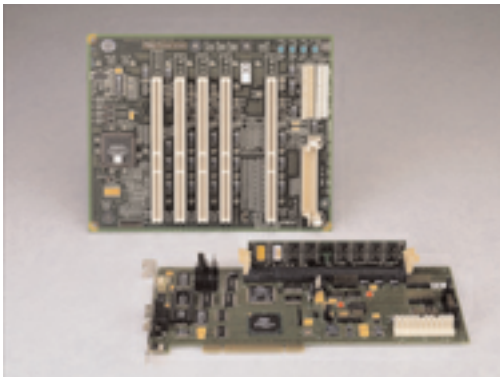
**The EBSA-285 Development Board At-a-Glance:**

EBSA-285 Evaluation Board is based on the PCI add-in card form factor, which can be used two ways:

- As the central processor in an SA-110-based computer, the EBSA-285 acts as the central processor, main memory, and host bridge and provides standard system capabilities, including interrupt controller, DMA controller, timers, and a UART. With the addition of a PCI backplane, the EBSA-285 can configure and control other devices on the PCI bus.
- As an add-in card in an existing PCI-based machine, the EBSA-285 acts as a coprocessor to the host system



*EBSA-285 Evaluation Board*



*EBSA-285 with Optional Backplane*

## SA-110 Microprocessor

The EBSA-285 is based on the SA-110 microprocessor, operating at speeds up to 233 MHz.

## 21285 Core Logic Chip

The 21285 is a highly integrated core logic controller for SA-110 microprocessor, performing all of the control functions on the EBSA-285. The device functions as a support chip for the SA-110 StrongARM microprocessor, integrating an SDRAM memory controller, PCI bus, UART (data leads only), timers, interrupt control, boot ROM/flash, and low-speed (X-Bus) I/O in a single device.

## Memory Subsystem

The EBSA-285 provides synchronous DRAM (SDRAM) for its main memory and flash ROM (with nonvolatile storage) for its boot path.

- The board includes two SDRAM DIMM sockets, with one 16 MB SDRAM DIMM supplied

## Memory Subsystem (continued)

- Four byte-wide 1 MB flash ROMs, provide non-volatile storage. The ROMs are arranged to provide a 32-bit ROM path

## I/O Subsystem

All local I/O within the EBSA-285 is programmed I/O under the control of the SA-110 microprocessor.

The I/O subsystem provides the following resources:

- An RS-232-C console port (COM0) with data-leads only that is accessed via a nine-way D-type connector on the bulkhead
- An 8-bit I/O port controls LEDs, reads the state of jumpers and contains a switch

## Interrupts

The EBSA-285 board can be used as a host bridge (e.g. when 21285 configured as the central function). In this case, logic in the 21285 chip acts as an interrupt controller for locally generated interrupts (generated on the module and within the 21285) as well as for interrupts generated by other devices on the PCI bus.

The EBSA-285 can also be used as an add-in card. In these applications, logic in the 21285 acts as an interrupt controller for interrupts generated locally (on the module and within the 21285). When used in this mode, the SA-110 microprocessor can generate an interrupt to the host bridge (across the PCI bus) under software control.

## PCI Interface

The EBSA-285 has a 32-bit PCI 2.1 interface that supports both 3.3-V and 5-V signaling.

## Clocks

The EBSA-285 uses two oscillators:

- The 3.6864-MHz oscillator drives the SA-110 phase-locked loop (PLL) input, enabling the SA-110 to generate its core clock. It also provides a fixed frequency input to one of the timers in the 21285 core logic device.
- The 50-MHz oscillator provides the osc clock input for the 21285. The 21285 buffers and redrives this clock to generate the SA-110 bus clock, the SDRAM clocks, and the 21285 feedback clock (fclk). The local buses and the majority of the chip's internal logic run synchronously at this clock frequency.
- The PCI clock is supplied by the backplane

## JTAG

The SA-110 and the 21285 both contain JTAG ports that allow test access to the I/O pins of the device.

## I/O Expansion

I/O can be expanded by the PCI interface and by expansion headers of the buffered 21285 X-Bus.

## PCI Backplane

The EBSA-BPL PCI passive backplane complements the EBSA-285 and enables developers to test a wide variety of StrongARM (and mixed processor) configurations.

Specifically, it allows verification and evaluation of the 21285 and future PCI-related StrongARM products as system masters and intelligent devices in desktop/server environments. The backplane provides the following capabilities:

- Supports all features on the EBSA-285 module
- Provides an environment for verification, evaluation, and benchmarking of StrongARM PCI support with the widest range of peripherals
- Enables the use of industry-standard enclosures and power supply units
- Provides an environment for testing current and future Intel PCI peripheral cards. Use with PCI bridge evaluation boards allows the investigation and verification of a wide variety of bridged bus configurations
- Provides 64-bit support

The PCI backplane includes five 64-bit PCI slots and is available in two configurations: EBSA-BPL-5V for the 5-V PCI signaling environment, and EBSA-BPL-3V3 for the 3.3-V PCI signaling environment.

## Software

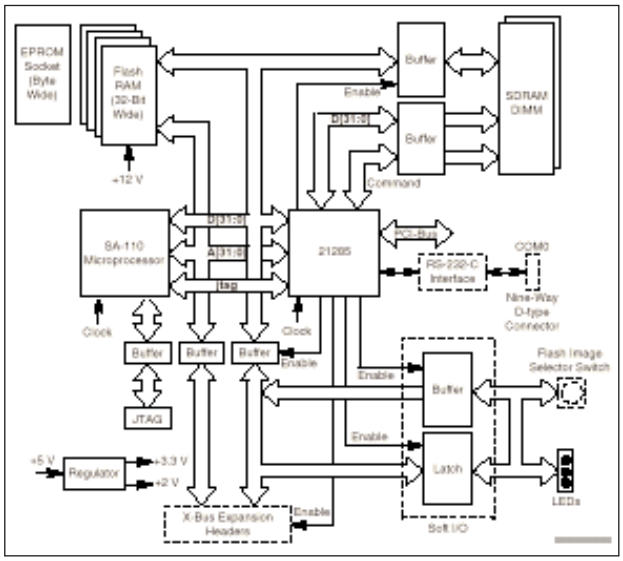
The EBSA-285 Evaluation Board supports a robust software environment:

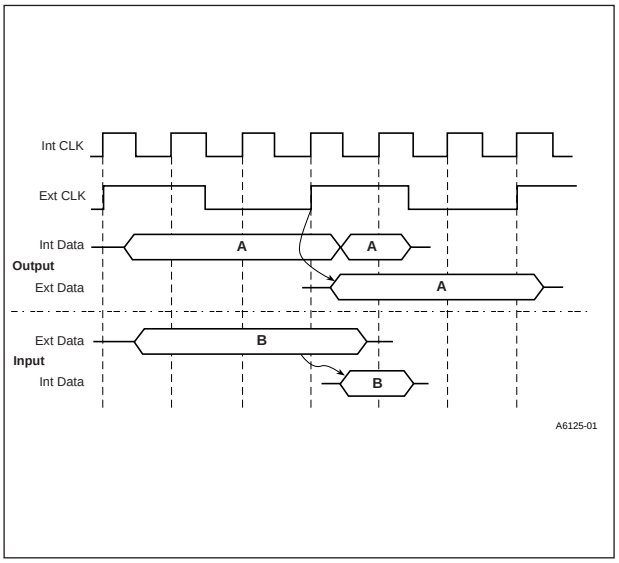
- Real-time operating systems include Nucleus+, ThreadX, µCOS, pSOS, C Executive, AMX, Linux, MQX/Kernel, Supertask!, VXWorks, NETBSD, eCOS, and µC/OS
- Software tools are available from ARM, Cygnus, Green Hills, ISI, Metaware, Microsoft, Microware, Wind River, and others

## SA-110/21285 Hardware Developer's Kit

The SA-110/21285 Hardware Developer's Kit documents non-proprietary designs that can be used for product development. The kit includes an *ARM Architecture Reference Manual, SA-110 Microprocessor Technical Reference Manual, StrongARM EBSA-285 Evaluation Board Reference Manual* and the following EBSA-285 code.

## EBSA-285 Block Diagram




**To order now**

Contact an authorized Intel distributor for complete ordering details.

- To order the EBSA-285 Evaluation Board, specify part number 21A85-01
- To order the 5V backplane for the EBSA-285, specify part number 21A85-02
- To order the 3.3V backplane for the EBSA-285, specify part number 21A85-03

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