PCI Development Backplane

User's Guide

October 1998

Order Number: 278149-001

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Introduction 1

1.1 Purpose

This manual describes the features, installation and configuration of Intel's custom PCI development backplane. The backplane allows a wide variety of StrongARM** (and mixed processor) topologies to be tested. Specifically, it will allow verification and evaluation of all 21285 PCI I/O support component and future PCI related StrongARM product line developments as system masters and intelligent devices in desktop/server environments.

1.2 Audience

The manual is intended for use by researchers, designers and developers who wish to experiment with or develop a variety of StrongARM-based system architectures using PCI as the primary interconnect mechanism.

1.3 Manual Organization

- Chapter 1, "Introduction", introduces the PCI development backplane and identifies its key features.
- Chapter 2, "Installation", provides general information on installation and connection of power.
- Chapter 3, "General Description", provides an overview of the backplane, explains the implementation of signals and identifies compatibility issues.
- Chapter 4, "Configuration", identifies and describes the configurable options and provides tables of jumper settings.
- Appendix A, "Technical Data", provides electrical and mechanical information about the backplane.
- Appendix B, "Layout and Circuit Diagrams", provides layout and circuit diagrams for completeness and to explain configuration options.
- Appendix C, "Bill of Materials", provides a combined bill of materials for the EBSA-BPL-5V and EBSA-BPL-3V3 Development Backplanes.

1.4 Conventions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

1.4.1 Caution

Cautions indicate potential damage to equipment or loss of data.

1.4.2 Note

Notes emphasize particularly important information.

1.4.3 Numbering

All numbers are decimal or hexadecimal unless otherwise indicated. The prefix 0x indicates a hexadecimal number. For example, 19 is decimal, but 0x19 and 0x19A are hexadecimal. Otherwise, the base is indicated by a subscript; for example, 100_2 is a binary number.

1.4.4 Signal Notation

In the circuit diagrams provided in Appendix B, active negative signals are indicated by a bar or overline; for example, $\overline{\text{FRAME}}$. Active positive signals have no bar.

Multiple signals are indicated by a colon and square brackets. For example AD[7:0] refers to address and data lines 7, 6, 5, 4, 3, 2, 1 and 0.

In text, active negative signals are suffixed by a # character. For example, IRDY#. Active positive signals have no suffix. This is consistent with the signal naming convention used in the PCI Local Bus specification.

1.5 Associated Documents

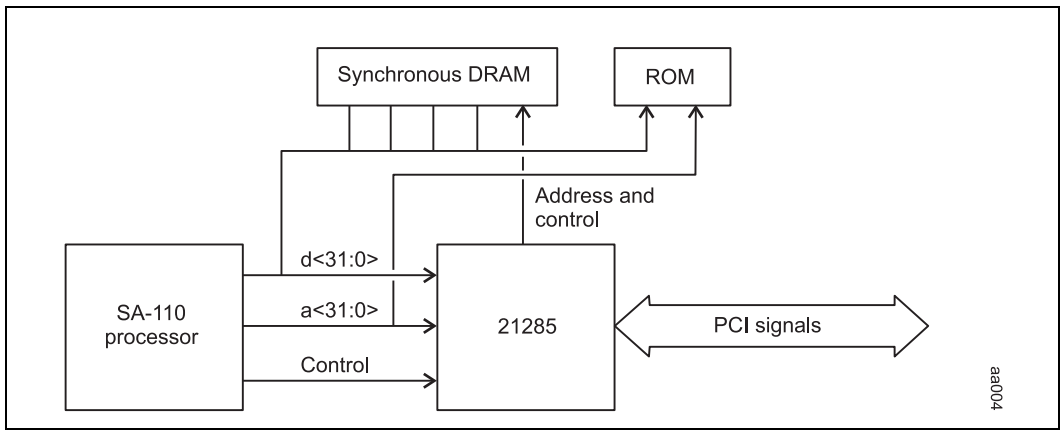
The following associated documents may be required or helpful when using this manual:

- *PCI Local Bus Specification*, Revision 2.1.
- *Cypress CY2260 datasheet* (available from **http://www.cypress.com**).
- Cypress application notes (*Crystal Oscillator Topics*, *Jitter in PLL-based Systems*, *Layout and Termination Techniques*). (all available from **http://www.cypress.com**)
- Intel AP-523 application note; *Pentium® Pro Processor Power Distribution Guidelines* (available from **http://www.intel.com** under Pentium® Pro processors). This application note describes the VRM module.
- *Semtech MP60 VRM Module Specification* (available from **http://www.semtech.com**).

1.6 StrongARM and PCI

The 21285 Core Logic Controller is part of Intel's provision of PCI I/O support for the StrongARM product family. Specifically, it is a support device for the SA-110 StrongARM microprocessor, integrating an SDRAM memory controller, PCI bus, DMA engine, UART (data leads only), timers, interrupt control, boot ROM/Flash and low speed (X-bus) I/O in a single device. The chip supports an optional system arbiter, which shares pins with the X-bus control signals making it an either/or option. Figure 1-1 shows a diagram of the 21285 and SA-110 in a Host Bridge application.

Figure 1-1. The 21285 in an SA-110 System

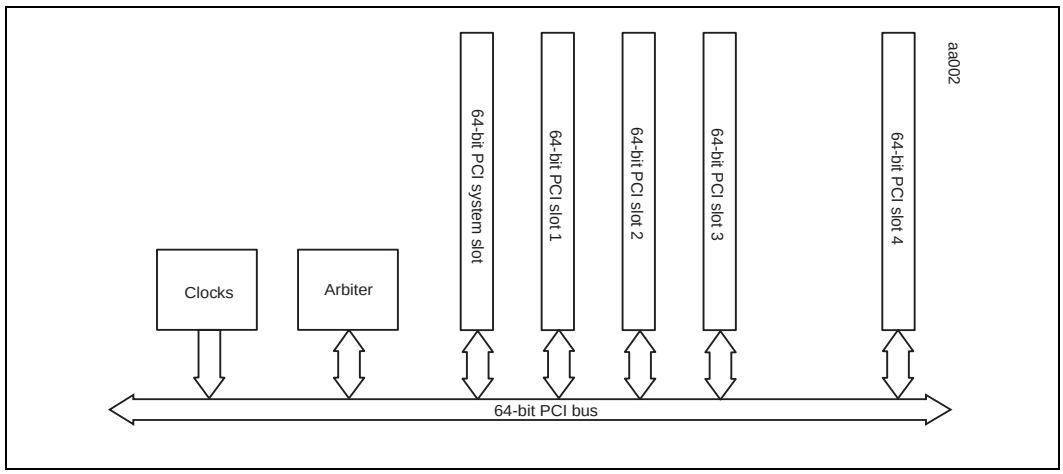


The 21285's PCI interface can be statically configured in one of two modes:

- As a device (configuration space enabled peripheral) on PCI
- As the system master (Host Bridge)

An evaluation board (EBSA-285) supporting both modes is available. It can also operate standalone where PCI is not required.This manual describes Intel's custom PCI backplane (Figure 1-2), which complements the EBSA-285 offering. The backplane allows a wide variety of StrongARM (and mixed processor) topologies to be tested. Specifically, it will allow verification and evaluation of the 21285 and future PCI related StrongARM product line developments as system masters and intelligent devices in desktop/server environments.

Figure 1-2. Backplane Block Diagram



1.7 Key Features

The backplane provides the following:

- Support for all features on the EBSA-285 module.
- An environment for verification, evaluation and benchmarking of StrongARM PCI support with the widest possible range of PCI peripherals. For this reason, the standard PCI I/O form factor adopted by the PC industry is used.
- The ability to use industry standard enclosures and PSUs.
- An environment suitable for testing all of Intel's current and future (standard form-factor assumed) PCI peripheral cards from the PPB, multimedia and communications business units with the StrongARM processor family. Of particular importance is interworking with the PCI bridge evaluation boards, allowing a wide variety of bridged bus topologies to be investigated and/or verified.
- 64-bit support (for future-proofing of the design).
- Two variants; EBSA-BPL-5V complying with the 5 V PCI signalling environment, and EBSA-BPL-3V3 with the 3.3 V PCI signalling environment.
- Backplane provision of the PCI system clock and PCI arbitration.
- Optional support of PICMG-style[1] arbitration from the system slot.
- Several link options have been provided to support different system configurations (see Section 4.2.1).

1. PICMG = PCI Industrial Computer Manufacturers Group. Please see their website (www.picmg.com) for more details.

Installation 2

2.1 Delivered Items

You should have received:

- This manual.
- Either backplane EBSA-BPL-5V (5 V signal levels) or EBSA-BPL-3V3 (3.3 V signal levels).
- A Voltage Reference Module (VRM). This may be separate, or it may be factory-fitted in connector J3.

With regard to installation, both boards are identical and will be installed in the same manner.

You will also need:

- Either a PC/AT chassis, or standoffs for mounting the PCB
- Either an AT-style PSU with +3.3 V output provision, or a standard AT-style PSU (+5 V, +12 V and -12 V only)[1]

Caution: If your PSU has a +3.3 V output that you wish to use, be sure to remove the VRM from the backplane BEFORE connecting power.

2.2 Preparation

The backplane offers several configuration options for selection by the user. The most likely of these have been preselected as defaults by links fabricated in the etch (etchlinks). It is expected that these will be used by the great majority of developers. Alternatives to the default options can be chosen by cutting the etchlinks and fitting header links as appropriate. As not all combinations of options may be fail-safe the user should read Chapter 4, “Configuration”, before modifying the board or applying power.

Caution: The backplane is a multilayer board. Take care not to damage etch or lower layers when cutting etchlinks. For more information, see Section 4.2.1.

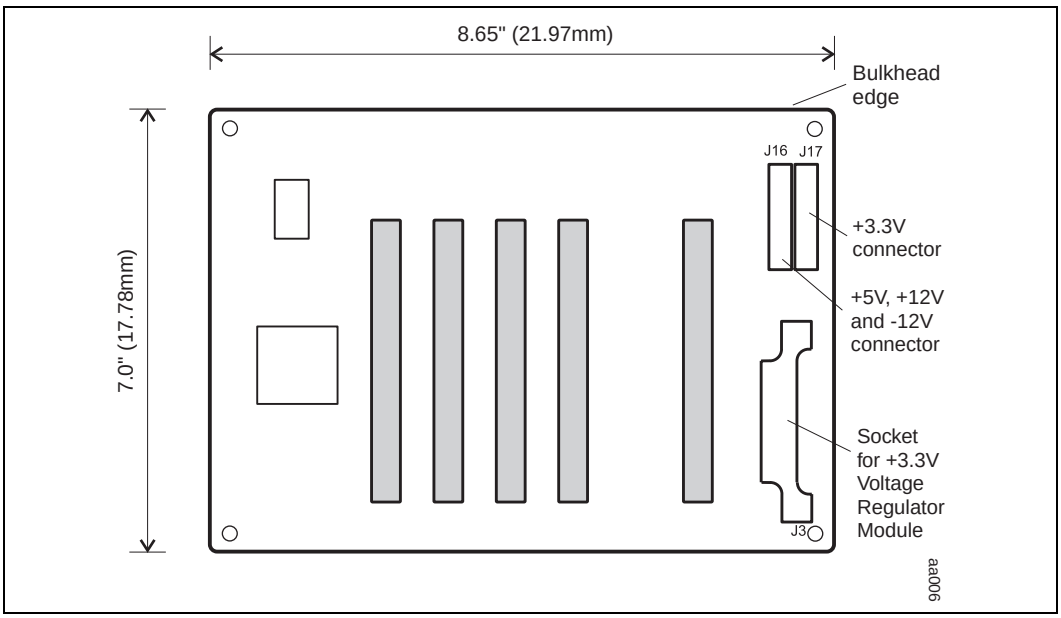
1. The -5V and DC_OK pins are not connected on the backplane.

2.3 Fitting the Board

Caution: Observe proper antistatic precautions when handling the board.

The board can be fitted in any standard PC/AT enclosure. Alternatively, it can be installed on pillars on the workbench. Board dimensions are shown in Figure 2-1.

Figure 2-1. Backplane Dimensions



2.4 Connection of Power Supplies

The board can be powered by **either** of two methods. Use either one, but **NOT** both.

- PC power supply with provision for +5 V, ±12 V and +3.3 V connected to J16 and J17.
- Standard PC/AT supply with +5 V and ±12 V connected to J16, and a +3.3 V Voltage Reference Module (VRM)[1] fitted in J3.

Note: J16 and J17 are standard PC motherboard power connectors. On J16, the -5 V and PWRGD pins are not connected.

Note: The current required by an EBSA-285 with 16 MB of SDRAM is typically 700 mA. This may be insufficient to reliably start some power supplies (PSUs). If you experience this problem, try increasing the load on the PSU by:

— adding cards to the backplane configuration

— attaching a disk to the PSU

— attaching a suitable load resistor (5 to 10 Ω, rated at 10W) to the +5 V line of an available disk power harness. **This should only be attempted by an appropriately qualified person.**

1. Both backplanes are fitted with a connector to accept the supplied Voltage Reference Module (VRM). Backplane circuitry configures the installed VRM to 3.3 V.

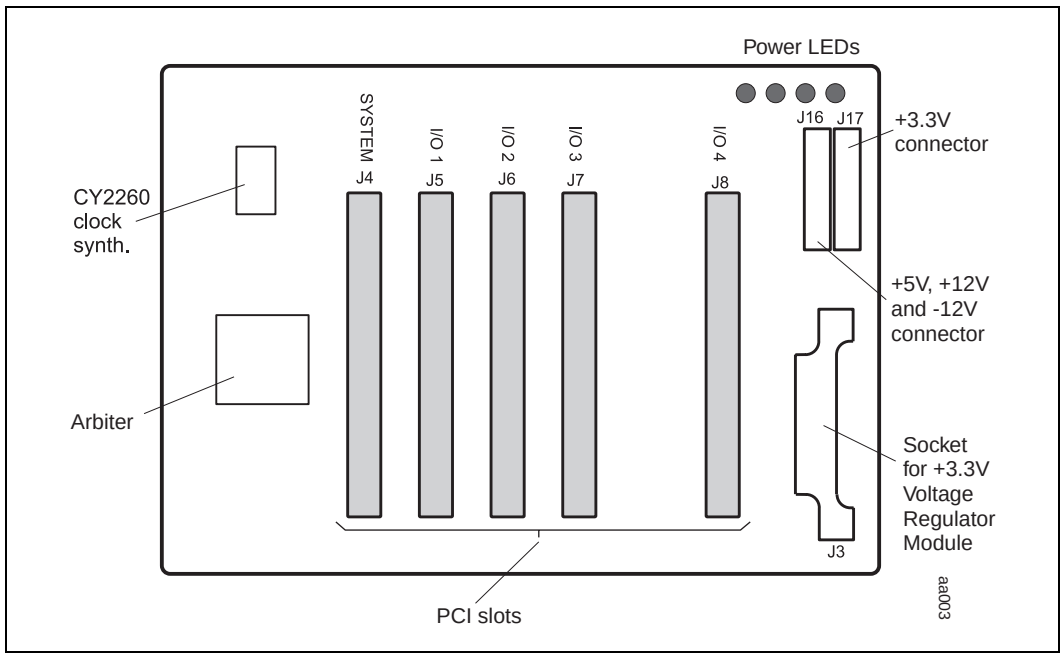
General Description 3

3.1 Overview

The backplane (Figure 3-1) is supplied in two versions; one for 5 V and one for 3.3 V signalling environments. The differences are:

- The PCI connector keying
- The voltage applied to the VIO power plane

Figure 3-1. Backplane Layout



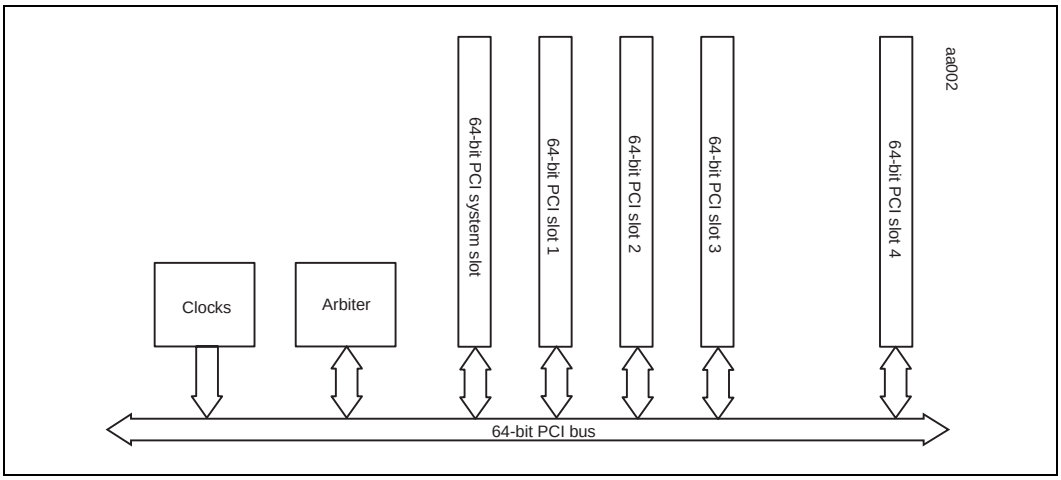
Both boards are compliant with the standard PC/AT outline and are drilled with common mounting holes allowing it to be fitted in generic eight-slot desktop or deskside enclosures. Five full-length 64-bit PCI slots are provided.

Depending upon the backplane model purchased, the PCI slots will support either 5 V or 3.3 V cards. Both will support universal cards.

An onboard clock synthesizer provides separate PCI clocks for the five PCI slots and an onboard arbiter.

A block diagram of the backplane is shown in Figure 3-2.

Figure 3-2. Backplane Block Diagram



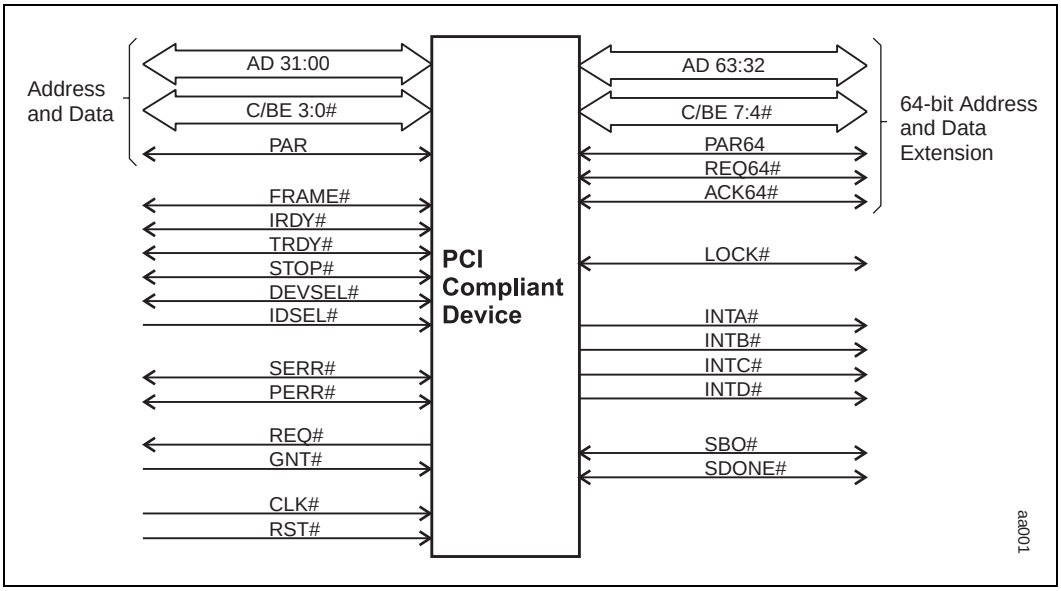
3.2 Signal Lines

This section describes the implementation of signal lines provided on the backplane.

3.2.1 General

The backplane provides all PCI signals except for JTAG boundary scan. The backplane implementation of the PCI bus is shown in Figure 3-3.

Figure 3-3. Backplane Implementation of PCI bus



All signal lines are bussed as parallel traces between all slots with the following exceptions:

- The interrupt lines.
- The request/grant arbitration lines.
- DEVSEL to the PCI I/O slots (J4-J7). DEVSEL does not apply to the system slot.
- PCI clocks.
- PRSNT bits. These are ac coupled to 0 V on each of the I/O slots as additional ac grounds.
- M66EN is tied to 0 V. The system is designed for 33 MHz operation only.

Pull-up resistors are provided on the following signals:

- SBO# and SDONE#
- REQ64# and ACK64#
- FRAME#, IRDY#, TDY#, STOP#, LOCK#, and DEVSEL#
- PERR# and SERR#
- INTA#, INTB#, INTC# and INTD#
- All arbiter request lines
- All 64-bit address and data extension lines

DEVSEL may be optionally coupled via links and a resistor to a choice of AD lines as follows:

- PCI I/O slot 1 - AD19 or AD31 (default AD19 via an etchlink)
- PCI I/O slot 2 - AD18 or AD30 (default AD18 via an etchlink)
- PCI I/O slot 3 - AD17 or AD29 (default AD17 via an etchlink)
- PCI I/O slot 4 - AD16 or AD28 (default AD16 via an etchlink)

See also the note on line numbering in Section 4.3.2.

3.2.2 Interrupts

Interrupt connections are ORed in such a sequence that any add-in I/O board using INTA# can be uniquely recognized by the system.

The interrupt lines are interconnected as shown in Table 3-1.

Table 3-1. Interrupt Line Connections

	pin6A	pin7B	pin7A	pin8B
System slot	INTA#	INTB#	INTC#	INTD#
I/O slot 1	INTB#	INTC#	INTD#	INTA#
I/O slot 2	INTC#	INTD#	INTA#	INTB#
I/O slot 3	INTD#	INTA#	INTB#	INTC#
I/O slot 4	INTA#	INTB#	INTC#	INTD#

3.2.3 Reset

RESET# must be provided by the system bridge device. No provision is made on the backplane for an external reset of the PCI. The arbiter will be reset asynchronously using this signal.

3.3 Arbitration

Bus arbitration can be controlled by the backplane or from the system slot. The arbiter algorithm is compliant with the *PCI Local Bus Specification*, Revision 2.1. For flexibility, this is implemented via a socketed PLD (Programmable Logic Device). The backplane arbiter fitted is based on an Altera Max 7000* series device in a 68-pin PLCC package.

The following signals are routed to and from all slots to the arbiter:

- A unique REQ# line for each slot with an external pullup
- A unique GNT# to each slot
- RESET#
- FRAME# and IRDY# to identify the bus idle condition
- LOCK# to identify resource lock cycles

In addition, the following backplane control inputs and monitoring outputs are provided:

- A bank of programmable CONTROL bits (1 per slot) defaulted high via pull-up resistors. These static control bits can be used as part of a 2-level priority or masking algorithm for the arbiter, assuming algorithm support. The algorithm shipped as standard does not use these inputs.
- An ARB_ENABLE# signal, which can be used to tri-state all outputs when an arbiter is provided by the system slot.
- A LOCK_ENABLE signal to allow the arbiter to optionally lock the bus on LOCK# cycles. This allows systems to switch between bus locked and resource locked configurations assuming the correct device support (hardware and/or software).
- Arbiter state monitoring outputs PCIARB[2:0] are brought out to a header for ease of connection to a logic analyzer etc.

3.4 System Clocks

System clocks are provided by a Cypress CY2260SC-3 clock synthesizer/driver and a 14.318 MHz crystal. The CY2260SC-3 has link options for 25 MHz, 27.5 MHz, 30 MHz and 33 MHz[1] support. This device provides six PCI clocks with low jitter, slew limiting, and maximum skew of <250 ps in a 28-pin SOIC package. All other clock outputs are unused.

There are no provisions for 66 MHz clocking.

1. Default - via an etchlink.

3.5 System Slot Compatibility Issues

Modules using the backplane arbiter must satisfy the following criteria:

- Provide CONFIG cycles to configure the four I/O slots
- Support the INT[A-D]# pins as inputs from the I/O slots as described in Table 3-1
- Provide PCI reset (RST#) for the system

In addition, modules providing PCI arbitration must use the system slot in the backplane and route the arbitration signals according to Table 3-2 and Table 3-3.

Table 3-2. System Slot Arbiter: PCI Pinout (Request)

Arbitrated slot	REQ		
I/O slot 1	18B	REQ#	($\overline{\text{SYSCPU\_REQ0}}$)
I/O slot 2	10B)	Reserved	($\overline{\text{REQ2}}$)
I/O slot 3	19A	Reserved	($\overline{\text{REQ3}}$)
I/O slot 4	9B	PRSNT1#	($\overline{\text{REQ4}}$)

Note: In the above table the first name is the name as specified in the PCI standard, the bracketed name is the signal name on the backplane.

Table 3-3. System Slot Arbiter: PCI Pinout (Grant)

Arbitrated slot	GNT		
I/O slot 1	17A	GNT#	($\overline{\text{SYSCPU\_GNT0}}$)
I/O slot 2	14A	Reserved	($\overline{\text{GNT2}}$)
I/O slot 3	26A	IDSEL	($\overline{\text{GNT3}}$)
I/O slot 4	11B	PRSNT2#	($\overline{\text{GNT4}}$)

Note: In the above table the first name is the name as specified in the PCI standard, the bracketed name is the signal name on the backplane.

Arbitration for the bus by the system slot module must occur within the card itself.

Note: The sharing of the grant pin and IDSEL can cause problems in systems that issue PCI configuration cycles in I/O slots. It is becoming common practice for intelligent I/O to interrogate the bus in this manner. System designs that use this backplane, and want to use system slot arbitration, must **NOT** tie the arbiter grant and IDSEL lines together on the module. It will not be possible for an I/O slot to interrogate the system slot with configuration cycles.

Configuration 4

4.1 Backplane Variants

Two variants with different PCI signalling voltages are available. Variant EBSA-BPL-5V provides 5 V signalling; variant EBSA-BPL-3V3 provides 3.3 V signalling. The choice of backplane purchased affects two features:

- PCI connector polarization
- VIO voltage level

Note: PCI signalling voltage is a factory set option. It is not user configurable.

4.1.1 EBSA-BPL-5V

On this backplane:

- The PCI connectors are keyed at pin positions 62/63 and 50/51.
- Soldered links W3 and W4 are fitted; W1 and W2 are not.

4.1.2 EBSA-BPL-3V3

On this backplane:

- The PCI connectors are keyed at pin positions 62/63 and 12/13.
- Soldered links W1 and W2 are fitted; W3 and W4 are not.

4.2 Configuration Options

Several backplane configuration options are available. These are related to:

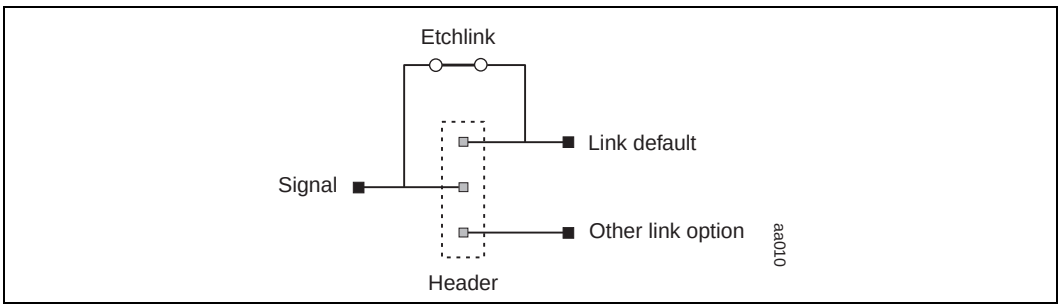
- Provision of a +3.3 V DC supply
- ID Select standard
- Arbiter source
- Clock frequency

The last three of these options are selected by etchlinks (see the following section) or header links.

4.2.1 Etchlinks

Etchlinks (links formed in the etch during fabrication) are used for selection of common defaults, with headers provided for jumper selection of other options. The etchlinks can be cut and jumpers fitted for verification modes, for example, switching between backplane and system-slot-based PCI arbitration. Figure 4-1 shows a general example.

Figure 4-1. Example of Etchlink

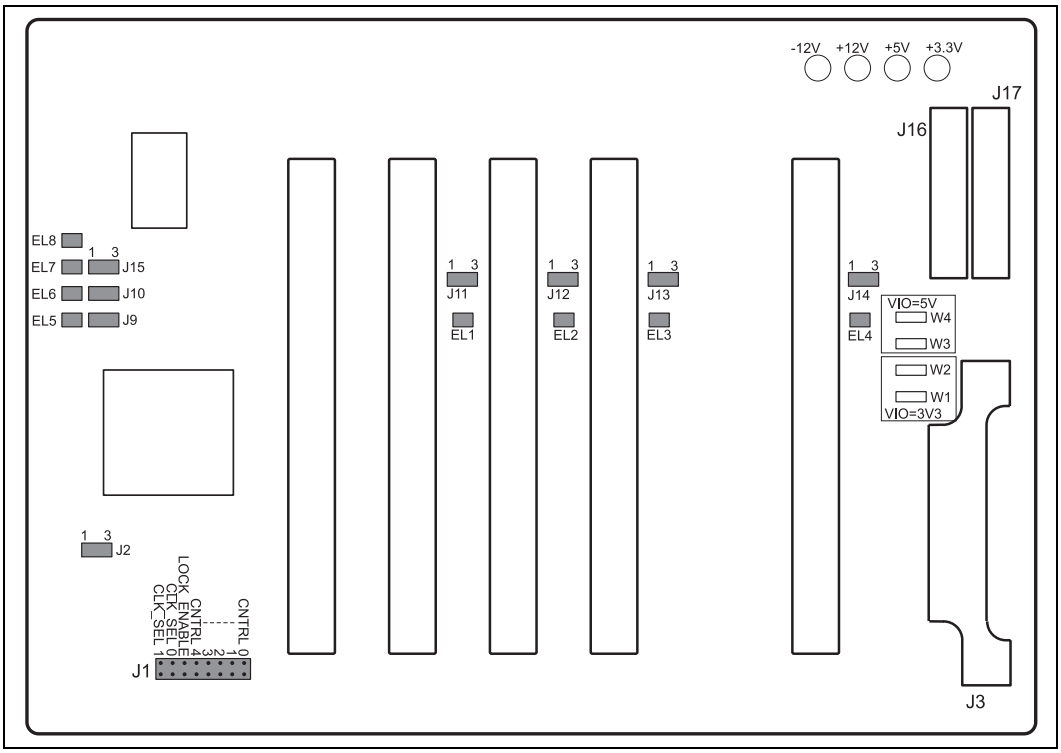


Etchlinks are all on layer 1 with plenty of trace clearance to allow them to be cut without risk of accidentally damaging other inner layer traces.

The available options will now be described. Refer to Figure 4-2 for component layout and to Appendix B for circuit diagrams. A set of quick reference configuration tables is provided at the end of this chapter.

Caution: If you use header links to select your options, make sure the associated etchlinks have been cut.

Figure 4-2. Etchlink and Header Locations



4.3 Configuring the Backplane

This section details the etchlinks to cut, and the jumpers to fit, for the desired method of operation.

4.3.1 Power Provision

Two mutually exclusive methods of power connection are available:

- PC/AT PSU to J16[1] and a 3.3 V Voltage Regulator Module (VRM) on J3
- PC/AT PSU with standard and 3.3 V outputs. Standard to J16[1] and 3.3 V to J17

Caution: J16 and J17 are weakly keyed. Take care to use the correct connector; the keying mechanism can be easily overridden.

Layouts, pinouts and PSU sleeve colors are shown in Figure 4-3.

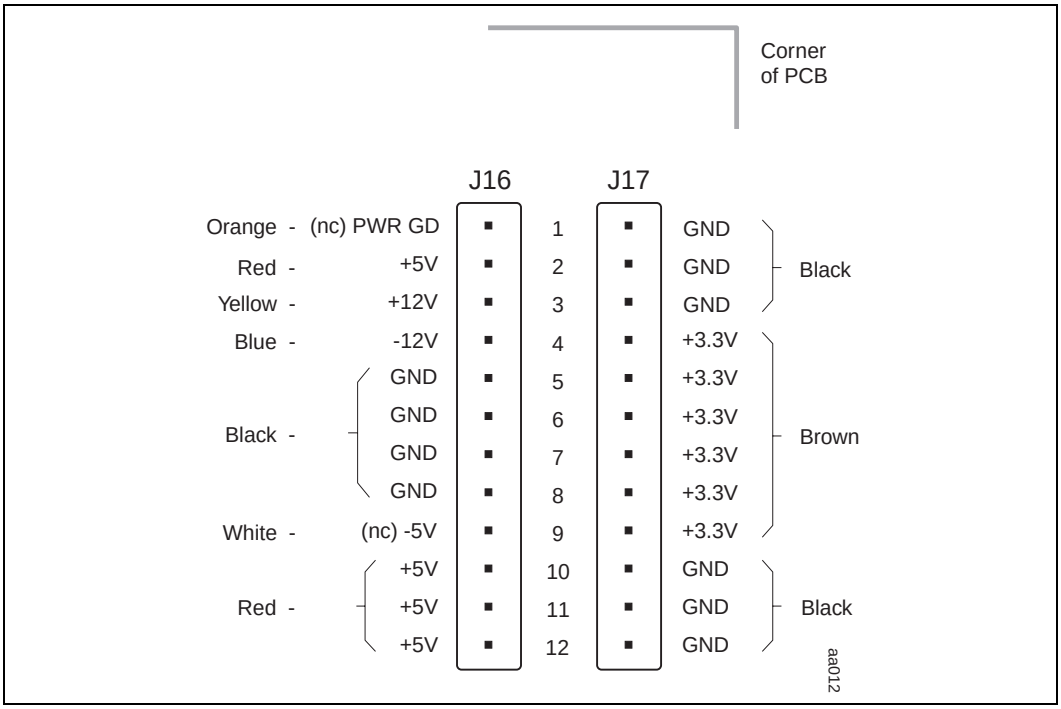
Note: The current required by an EBSA-285 with 16 MB of SDRAM is typically 700 mA. This may be insufficient to reliably start some power supplies (PSUs). If you experience this problem, try increasing the load on the PSU by:

— adding cards to the backplane configuration

— attaching a disk to the PSU

— attaching a suitable load resistor (5 to 10 Ω, rated at 10 W) to the +5 V line of an available disk power harness. **This should only be attempted by an appropriately qualified person.**

Figure 4-3. Power Connector Details



1. Industry standard connector supplying +5 V and ±12V (the -5 V and PWRGD pins are not connected).

4.3.2 ID Select

On the PCI bus, AD19:16 are normally used for IDSEL#. However, the PICMG[1] standard specifies AD31:28. Provision for both is made on the board. By default, AD19:16 are etchlinked to IDSEL#. If the etchlinks are cut for any reason, this same selection can be made by jumpering 2-3 on J11 to J14. For the PICMG standard, cut etchlinks EL1 to EL4, and install jumpers on J11 to J14, position 1-2.

Note: The PICMG standard specifies decrementing address line numbering with incrementing slot numbers. This is the convention adopted in the backplane labelling; however, it can be very confusing for those unaware of the issue when developing PCI configuration code.

4.3.3 Arbiter

The onboard arbiter allows the backplane to provide arbitration for the PCI bus.

4.3.3.1 Arbiter Source

Bus arbitration can be controlled from either the backplane arbiter (default) or the system slot.

Etchlinks on system-slot GNT# (EL7), system-slot REQ# (EL6) and ARB_ENABLE# (EL5) select the backplane arbiter. If the etchlinks are cut for any reason, this same selection can be made by jumpering 1-2 on J9, J10 and J15.

To use a system slot arbiter, cut etchlinks EL5-7 and fit jumpers on 2-3 of J9, J10 and J15. All three links (slot 0 grant routing, slot 0 request routing, and arbiter enable) need to be changed in unison.

4.3.3.2 Lock

LOCK_ENABLE is a control signal for the arbiter. It is pulled high by default.

4.3.3.3 Arbiter Algorithm

For developers who may wish to use their own arbitration algorithms, five optional control inputs (CNTRL 0 to 4) are made available for grounding on J1. All are pulled high by default.

4.3.4 Clock Frequency

S0 and S1 are the PCI clock speed select lines for the CY2260 clock synthesizer. Both have pullups. Options are 25 MHz, 27.5 MHz, 30 MHz and 33 MHz.

Etchlink EL8 grounds S1 (CLK_SEL 1), defaulting the bus clock to 33 MHz. If EL8 is cut, 33 MHz is selected by a jumper on header J1, CLK_SEL 1.

To select 25 MHz, cut the etchlink and fit jumpers on headers J1, CLK_SEL_0 and 1.

For 27.5 MHz, simply cut the etchlink.

For 30 MHz, cut the etchlink and fit a jumper on header J1, CLK_SEL 0.

1. PICMG = PCI Industrial Computer Manufacturers Group. Please see their website (www.picmg.com) for more details.

4.4 Quick Reference Configuration Tables

The following tables summarize the configurable options provided on the backplane. See Section 4.3 for a more detailed description.

Caution: ID select lines, arbiter source and clock frequency defaults are set by etchlinks. Do not use header links unless the associated etchlinks have been cut. Table 4-1 to Table 4-4 assume that the associated etchlinks have been cut.

Table 4-1. Power Connector Combinations

PSU type	Connect to J16	Connect to J17	VRM on J3
PC/AT	YES	NO	YES
PC/AT with +3.3V provision	YES	YES	NO

Table 4-2. IDSEL Configuration

	Hdr Link in Position 1-2	Hdr Link in Position 2-3
J11	AD31	AD19 *
J12	AD30	AD18 *
J13	AD29	AD17 *
J14	AD28	AD16 *

* Default - via EL1, 2, 3 and 4

Table 4-3. Selection of Arbiter Source

Arbiter	J9 ($\overline{\text{ARB\_ENABLE}}$)	J10 (REQ 0/1)	J15 (GNT 0/1)
Backplane *	Link position 1-2	Link position 1-2	Link position 1-2
System	Link position 2-3	Link position 2-3	Link position 2-3

* Default - via EL5, 6 and 7

Table 4-4. Selection of Clock Frequency

Frequency	CLK_SEL 0	CLK_SEL 1
25 MHz	IN	IN
27.5 MHz	OUT	OUT
30 MHz	IN	OUT
33 MHz *	OUT	IN

* Default - via EL8

Technical Data A

A.1 Electrical Data

The backplane complies with the *PCI Local Bus Specification*, Revision 2.x, thereby making the design as flexible as possible:

- The larger connectors provide a 64-bit PCI environment.
- 5 V or 3.3 V signalling versions available, with a VIO signal plane to provide the appropriate voltage to the connector VIO pins, the active logic, and associated pullups.
- Programmable backplane arbiter provided on socket U1. This is implemented in an Altera MAX 7000* device operating at 5 V but with separate I/O power pins that can operate at 5 V or 3V3.
- Low skew, slew limited system clocks to all slots and the backplane arbiter. The system clock generator is based on a Cypress CY2260-3 clock synthesizer/driver which provides six compliant PCI clock pins. The CY2260 can operate from 5 V or 3.3 V.
- +5 V, +12 V and -12 V supplies from an industry standard PC/AT PSU are connected via J16. PowerOK and -5 V from the power supply are not used.
- +3.3 V can either be supplied on industry standard connector J17 from a power supply unit, or it can be converted down from +5 V by a 3.3 V Voltage Reference Module (VRM) connected to J3. These two options are mutually exclusive. A warning to this effect is silk-screened onto the board.

A.2 Mechanical Data

The board is mechanically compliant with standard PC/AT outline (smaller size, using a subset of the mounting holes), allowing it to be fitted to generic 8-slot desktop or deskside enclosures. Five full-length 64-bit PCI slots are supported (no motherboard component restrictions). The PCI connectors support 5 V, 3.3 V or mixed voltage cards according to the backplane variant purchased.

The five slots occupy an 8-slot AT card enclosure (reading from right to left as viewed from the rear of the enclosure) as follows:

- slot 0 - empty - no connector
- slot 1 - empty - no connector
- slot 2 - system slot
- slot 3 - PCI I/O slot 1
- slot 4 - PCI I/O slot 2
- slot 5 - PCI I/O slot 3
- slot 6 - empty - no connector
- slot 7 - PCI I/O slot 4

This maximizes access to the component side of the system and one I/O slot for logic analyzer attachment, probing, daughtercards, etc.

Note: Due to the height of components, the EBSA-285 PCI Development Board occupies two slots of an AT motherboard. On the backplane, space is provided to the left of the system-slots and I/O4-slots to allow the EBSA-285 to be installed in either of these positions without sacrificing one of the other slots.

A.3 Construction

The backplane is an 8-layer board with the following layer makeup:

- Component side - pads, etchlinks and dispersion etch only
- VIO - power plane
- Signal layer 1
- +3.3 V plane
- GND plane
- Signal layer 2
- +5 V power plane
- Solder side - pads only

A.4 Test Points

For ease of connection to power and ground planes, a range of through-plated holes to take 0.025 inch (0.635 mm) square-posts, is provided for the construction of test points. These are not shown on the schematics but are silk-screened on the etch. The following test point positions are provided:

- GND TP1 to GND TP9
- VIO TP1 to VIO TP4
- VDD TP1
- 3V3 TP1

Layout and Circuit Diagrams B

This appendix contains layout and circuit details of the PCI backplane.

Figure B-1. Backplane Arrangement in a PC/AT Chassis

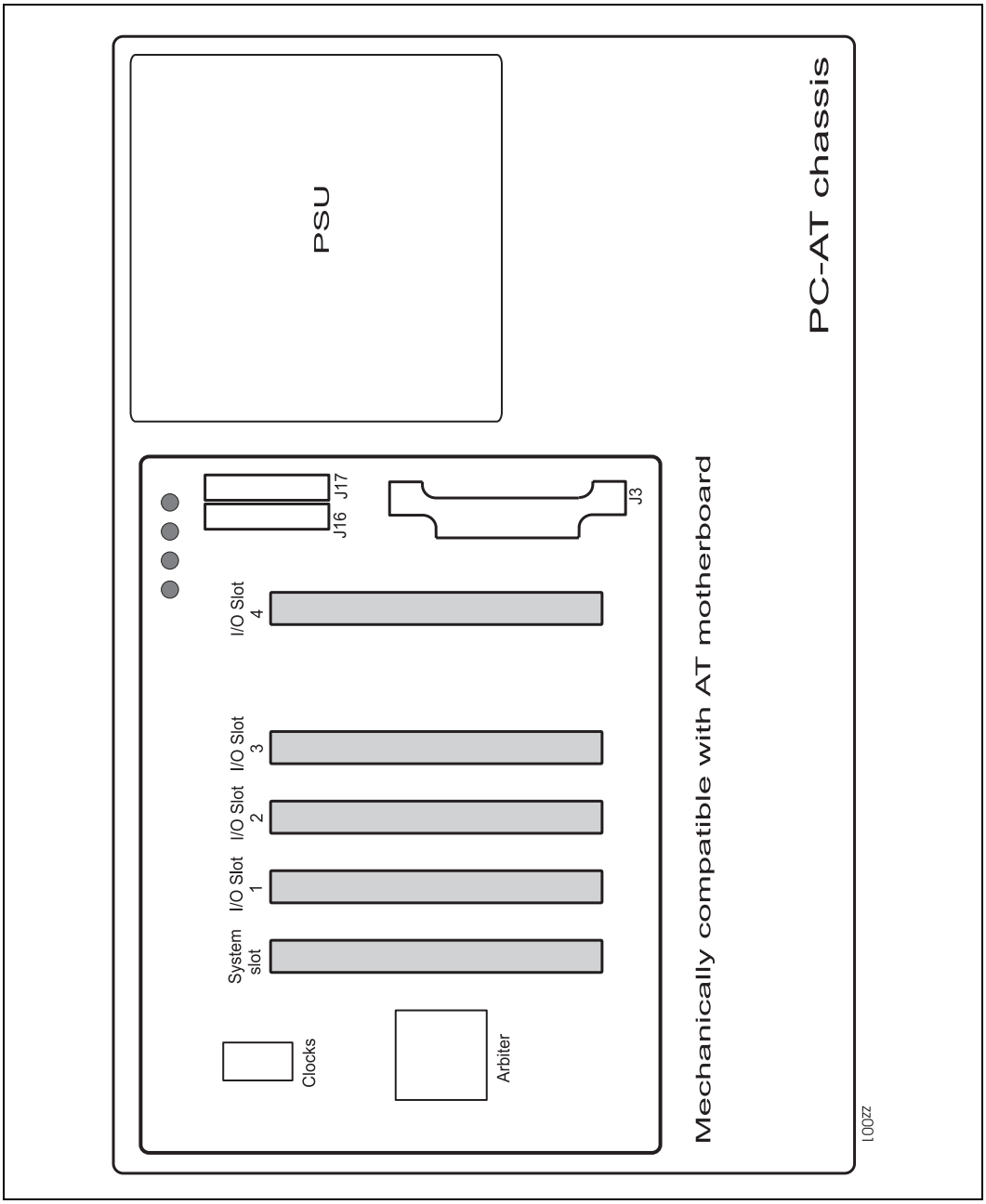
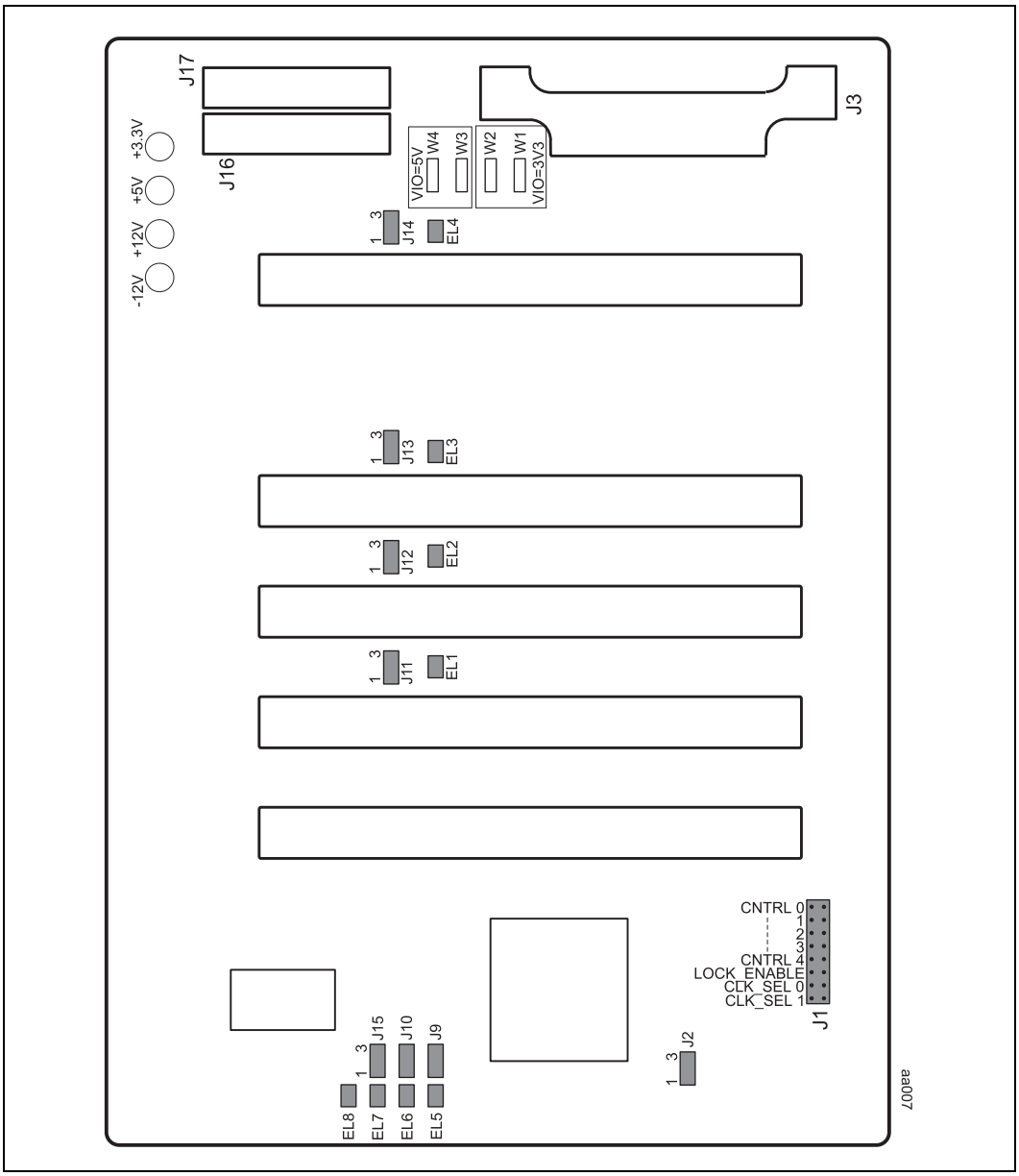


Figure B-2. Jumper and Connector Locations



B.1 Movable Keys

In Figures B-3 through Figure B-7, the 3.3 V key, which is referenced as *3.3V Key*, and the 5V key, referenced as *5V Key*, allows the module to be configured for either 3.3V or 5V enviroments, but not both. The 3.3 V key is located between pins 106 and 107 on side 2, and pins 12 and 13 on side 1. The 5 V key is located between pins 144 and 145 on side 2, and 62 and 63 on side 1.

Figure B-3. Circuit Diagram: System Slot

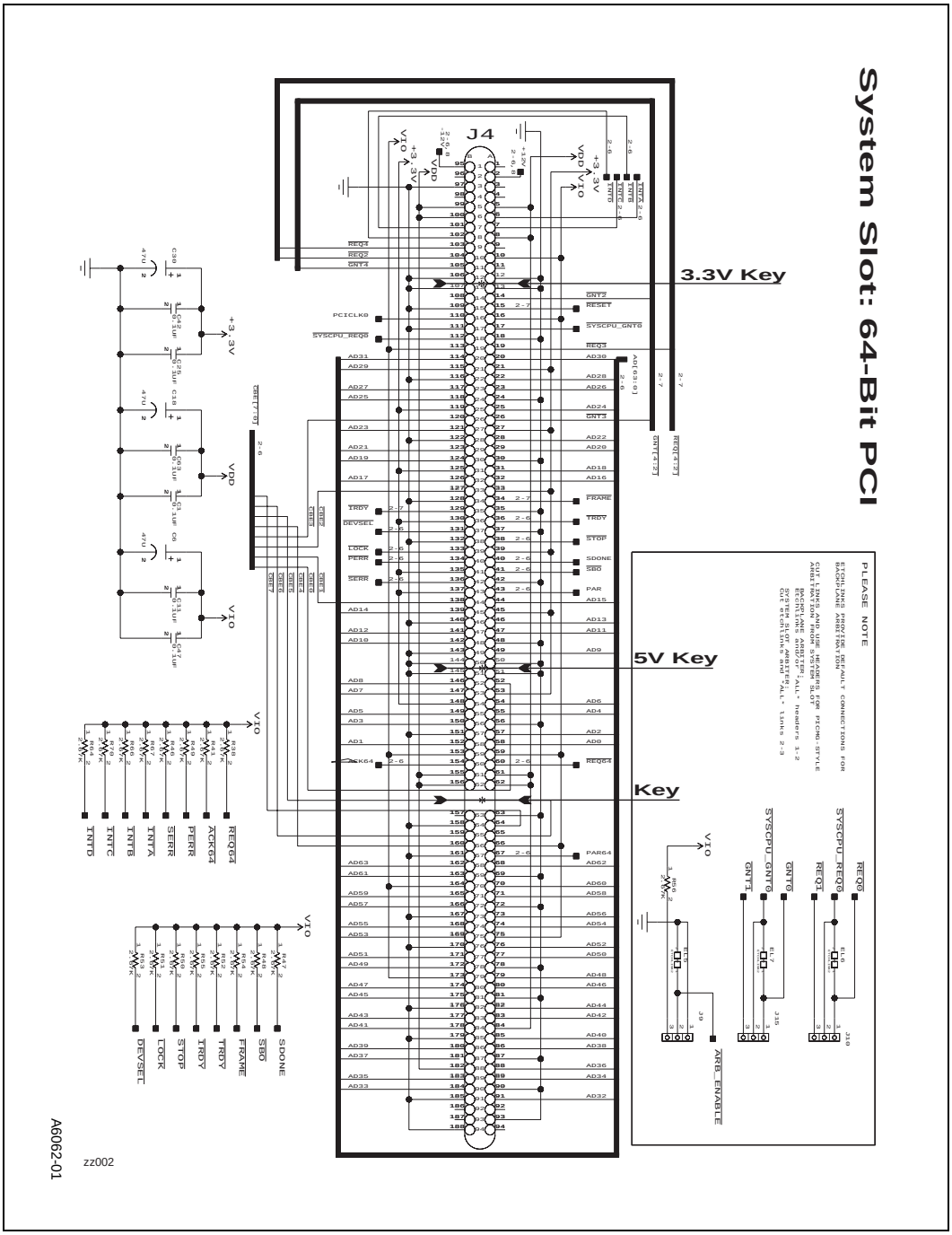


Figure B-4. Circuit Diagram: Slot 1

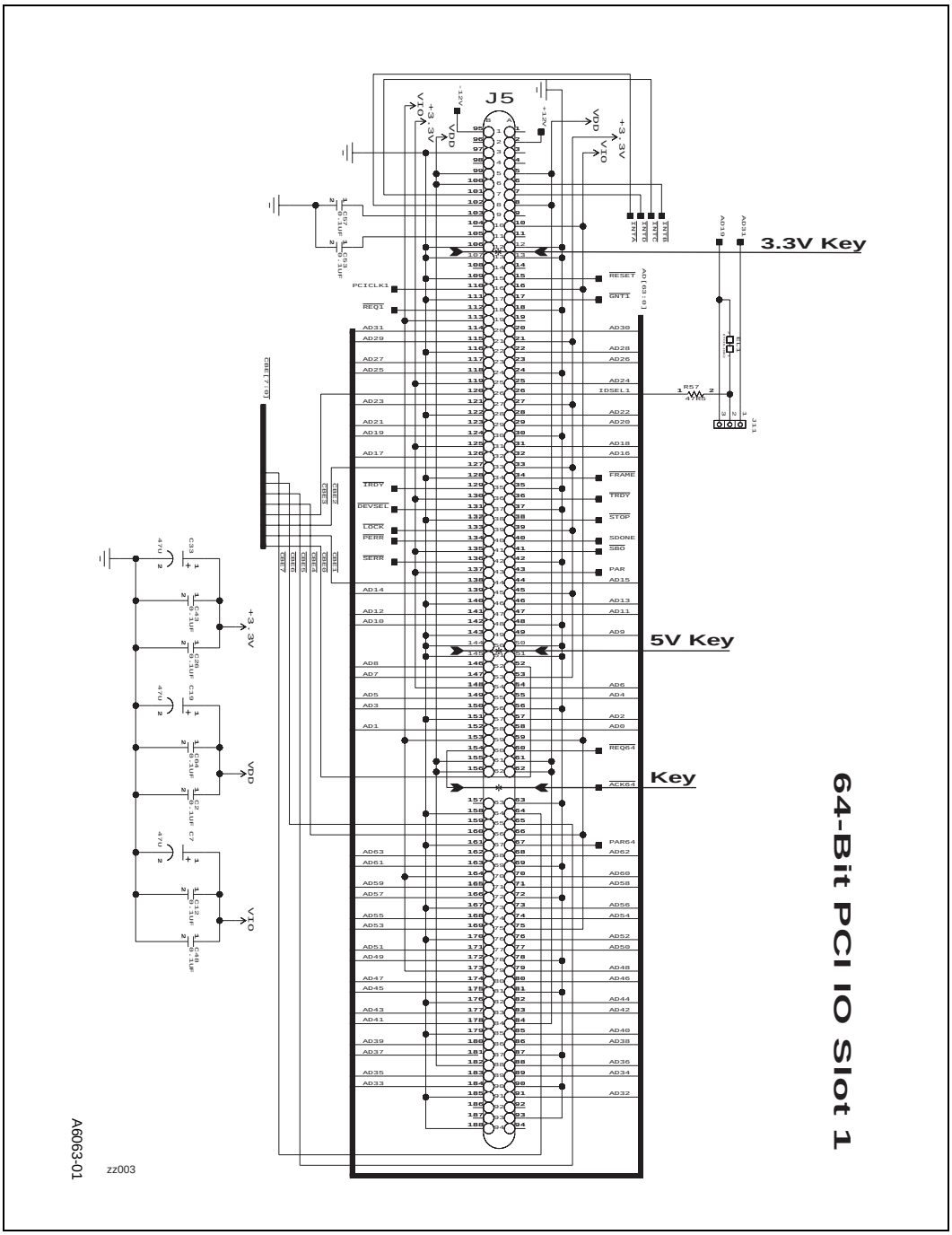


Figure B-5. Circuit Diagram: Slot 2

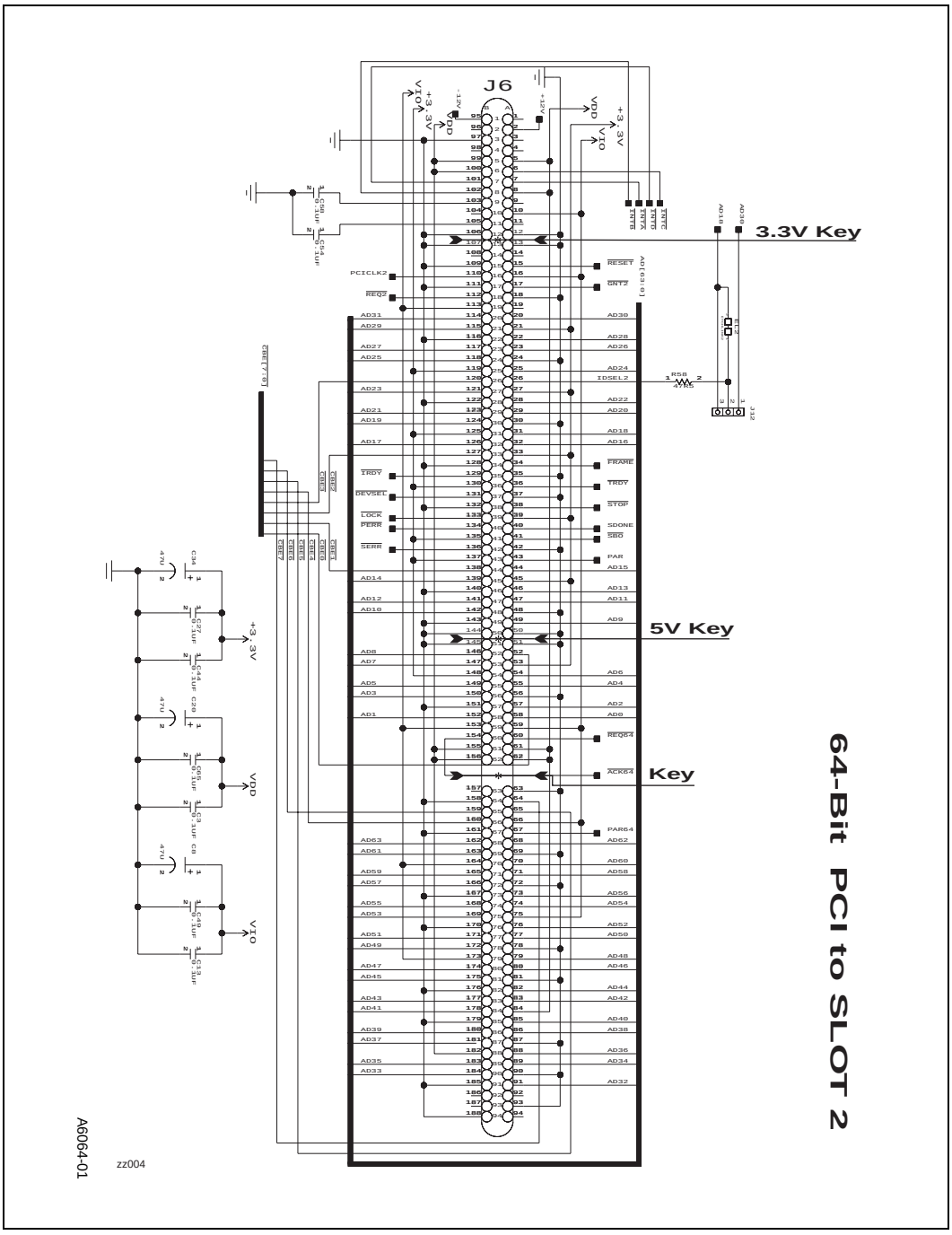


Figure B-6. Circuit Diagram: Slot 3

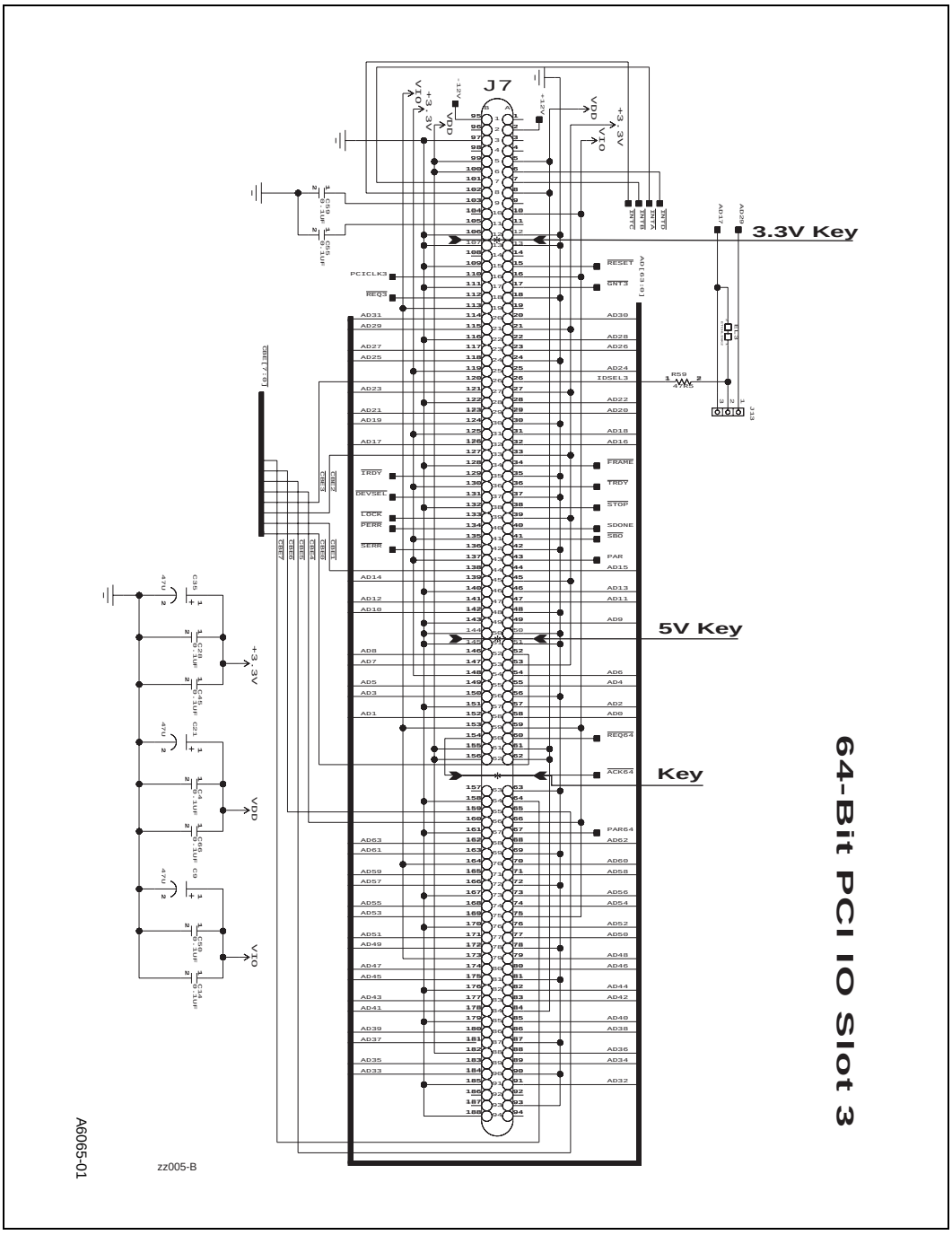


Figure B-7. Circuit Diagram: Slot 4

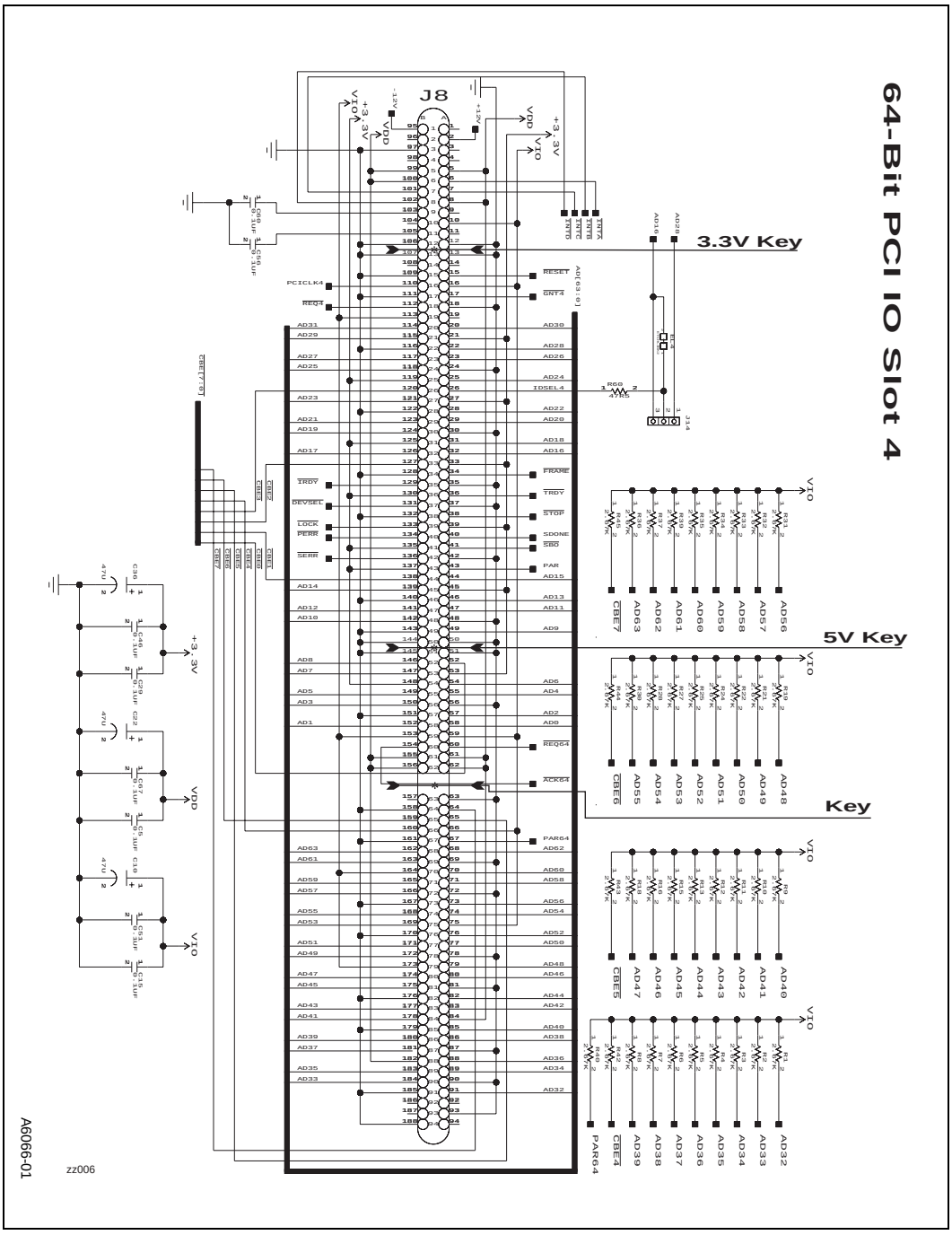


Figure B-8. Circuit Details: Arbitration and System Clock Logic

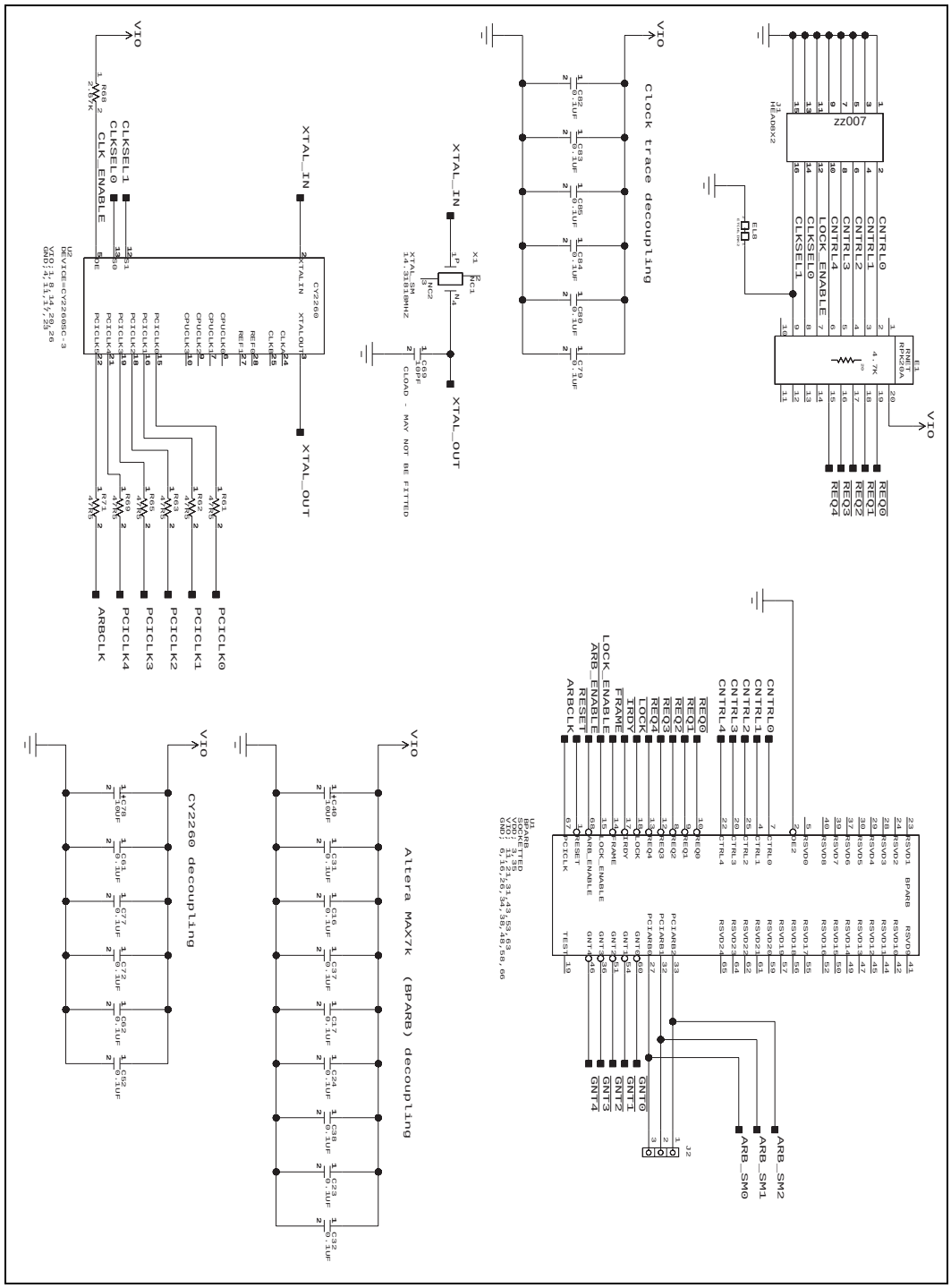
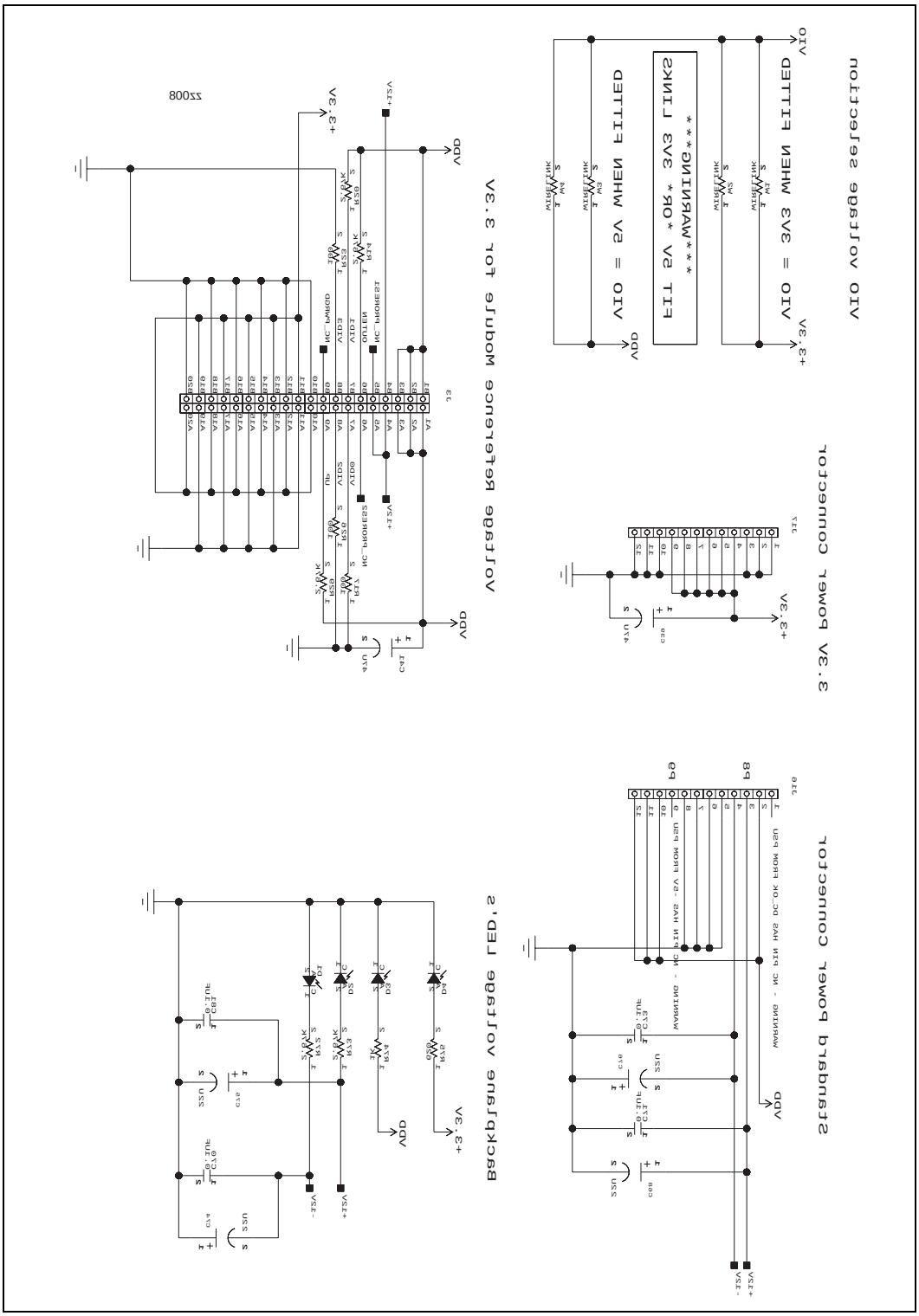


Figure B-9. Circuit Details: Power Connectors



Bill of Materials C

A combined bill of materials (Figure C-1) for the EBSA–BPL–5V and EBSA–BPL–3V3 Development Backplanes is given on the next page.

Figure C-1. Bill of Materials

						EBSA-BPL-xxx: Bill of Materials		
Item	Usage		Part No.	Manufacturer	Part No.	Description	Ref. Designators	
	BPL-5V	BPL-3V3						
1	1	1	10-24051-69			100V 5% 10pF NPO (0805 pkg)	C69	
2	61	61	10-24053-34			50V 20% 0.1uF Z5U (0805 pkg)	C1-5, C11-17, C23-29, C31-32, C37-38, C42-67, C70-73, C77, C79-85	
3	2	2	10-34976-21	Sprague	293D106X9016C2T	16V 20% 10uF tantalum (C pkg)	C40, C78	
4	4	4	10-34976-25	Sprague	293D226 X0020D2T	20V 20% 22uF tantalum (D pkg)	C68, C74-76	
5	17	17	10-34976-27	Sprague	293D476 X0016D2T	16V 20% 47uF tantalum (D pkg)	C6-C10, C18-22, C30, C33-36, C39, C41	
6	4	4	11-29934-01	HP	HLMP-4740	LED - green	D1-4	
7	1	1	12-13488-13	AMP	102977-8	8x2 unshrouded header	J1	
8	8	8	12-15901-08	AMP	102976-3	3 x 1 header	J2, J9-15	
9	A/R	A/R	12-18783-02	AMP	880584-2 or 382811-6	jumper	as required (items 7 and 8)	
10	1	1	12-32911-05	AMP	822280-1	EPLD socket - 68 pin PLCC	XU1	
11	1	1	12-38878-01	Molex	87218-1202	1 x 12 AT power connector (5V etc.)	J16	
12	1	1	12-38878-03	Molex	87218-1205	1 x 12 AT power connector (3.3V)	J17	
13		5	12-39839-07	AMP	145168-4	64 bit PCI conn - 3V3 keyed	J4-8	
14	5		12-39839-09	AMP	145169-4	64 bit PCI conn - 5V keyed	J4-8	
15	1	1	12-45158-02	AMP	146315-1	VRM 3.3V power module conn	J3	
16	1	1	13-30127-01	Bourns	4820P-002-472	19 x 4k7 resistor pack	E1	
17	10	10	13-35791-66			E96 47.5R 0.1W 1% (0805 pkg)	R57-63, R65, R69, R71	
18	3	3	13-35792-01			E96 100R 0.1W 1% (0805 pkg)	R17, R23, R26	
19	1	1	13-35812-01			E96 1k 0.1W 1% (0805 pkg)	R74	
20	60	60	13-35812-42			E96 2.67k 0.1W 1% (0805 pkg)	R1-16, R18-22, R24-25, R27-56, R64, R66-68, R70, R72-73	
21	1	1	13-42645-44			E96 620R 0.1W 1% (0805 pkg)	R75	
22	1	1	18-33643-10	Seiko	MA506 50/30/20/20	14.318MHz Xtal	X1	
23	1	1	21-45656-01	Cypress	CY2260SC-3	Clock synthesizer/driver	U2	
24	1	1	23-000YW-01	Altera	EPM7064LC68-12	PLD - bparb	U1	
25	1	1	50-20725-01		n/a	PCB		
26		2	90-09185-00		CR-25 compatible pkg	0 ohm 'resistor' - axial	W1, W2 (ties VIO => 3.3V)	
	2					...contd.	W3, W4 (ties VIO => 5V)	

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