Setting Up the Intel® StrongARM® SA-1111 Companion Chip for DMA Access to SDRAM

Application Note

August 1999

Order Number: 278296-001

Application Note

Contents

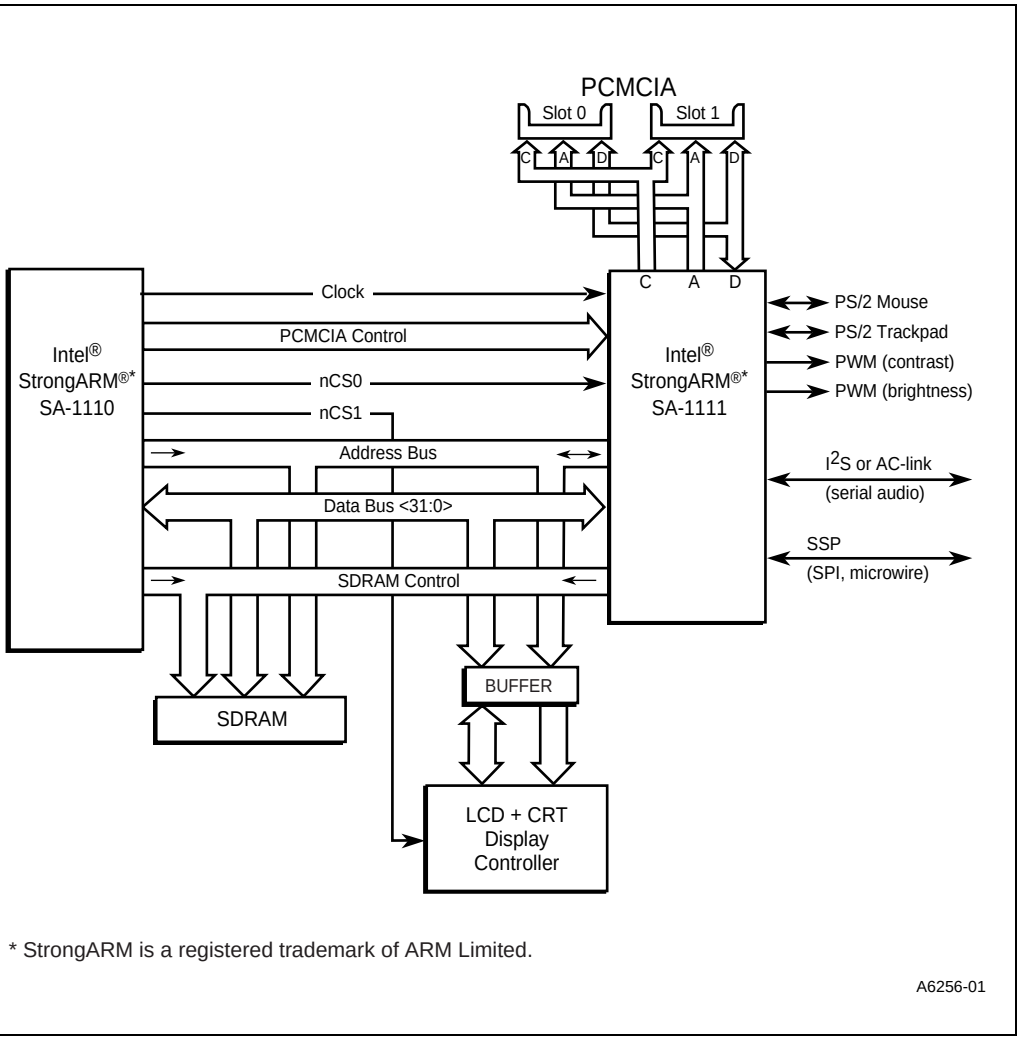
Figures

Tables

1.0 Overview

The Intel® StrongARM® SA-1110 processor (SA-1110) and the Intel® StrongARM® SA-1111 companion chip (SA-1111) are both connected to and share access to system main memory. The main memory is comprised of one or more physical banks of SDRAM (Synchronous DRAM). Normally the SA-1110 processor controls the SDRAM for functions such as cache load and store, DMA to and from processor peripheral ports, and LCD display refresh. The SA-1111 can also access one bank of SDRAM. This enables the SA-1111 to directly transfer data between system memory and its USB Host Controller or Serial Audio Controller units.

Figure 1. Types of SDRAM Access



The use of DMA for these transfers avoids multiple moves of data across the system bus using Programmed I/O (PIO), and takes advantage of the inherent high-bandwidth capabilities of SDRAM. It also unloads the SA-1110 processor of the burden of word-by-word management of data transfers between SA-1111 subsystems and main memory. The high bandwidth of DMA, and the unloading of the SA-1110 processor so it can perform other duties results in higher overall system performance.

1.1 Signal Interconnect

The SA-1111 connects to the main system bus of the SA-1110 processor, including a data bus, an address bus, and a variety of control lines. Included in this signal set are all the signals required to control one bank of the system's main memory SDRAMs. This permits either device to control the memory. The signals include:

- 32-bit data bus
- 15 bits of the 26-bit address bus
- nSDRAS, nSDCAS, nSDCS (Chip Select), SDCLK (Clock), nWE (Write Enable)

Note: SDCKE (Clock Enable) is always driven by the SA-1110.

1.2 DMA Controllers

The two blocks on the SA-1111 that take advantage of DMA are the USB Host Controller and the Serial Audio Controller. DMA permits large blocks of data to transfer automatically (from the SA-1110 processor point of view), once the transfer has been set up by the processor.

Each of the two subsystems has a simple DMA controller built in. Registers permit the processor to specify a starting address in SDRAM, and a transfer length. The Audio Controller additionally permits two buffers to be set up in memory for each direction of transfer, so that one buffer can be actively transferring while the second buffer is being set up. This permits continuous streams of data in both directions. Small FIFOs on the SA-1111 buffer the data locally, to match the "bursty" high-bandwidth transfer characteristics of SDRAMs with the much slower steady data stream at the USB or audio pins.

1.3 Shared Memory Controller

In addition to the DMA controllers, the SA-1111 has a memory controller (SMC – Shared Memory Controller). When one of the device's DMA controllers wants access to system memory, it sends a request to the SMC. The SMC in turn requests the external memory bus (using signal MBREQ), and the SA-1110 responds – when it is ready to give up control of the memory – with MBGNT, and tristates (off) all signals to memory. The SMC begins to drive memory address and control signals, and tells the original requester (USB or Audio controller) that it can begin memory transfers. The controller begins data transfers across the internal memory bus, and the SMC translates those transfers into SDRAM cycles.

The SMC must be set up correctly before accessing SDRAM. There are several parameters that must be set:

- DRAM type
- Row address width
- CAS latency (SDRAM only)

In general, the bit descriptions and required values are identical to the corresponding bits in SA-1110 Memory Controller registers. They should be set to identical values to ensure correct operation.

1.3.1 DRAM Type (Register SMCR, Bit 0 – DTIM)

The DRAM type, which is specified in the DTIM bit of the SMCR register, is set to a“1” for SDRAM.

Note: The DTIM register on the SA-1111 must be set to the same value as the DTIM register on the SA-1110.

1.3.2 Row Address Width (Register SMCR, Bits 4:2 – DRAC)

The DRAC bits specify the number of Row Address bits required for the particular SDRAM used in the system. Value 001 = 10-bit row address, value 110 = 15-bit row address. The default power-up value is 101 = 14-bit row address. Table 1 shows the row address width for all SDRAMs likely to be used in a system. The term “row address width” includes all internal bank address bits. SDRAMs always have one or two internal bank address bits, designated BA[0] or BA[1:0].

Table 1. DRAM Address Configuration and Register Settings

DRAM Size	DRAM Organization	Address Row and Column Width	DRAC Setting
16 Mbit	1M x 16	10 x 10	001
		12 x 8	011
	2M x 8	11 x 10	010
		12 x 9	011
	4M x 4	11 x 11	010
		12 x 10	011
64 Mbit	4M x 16	11 x 11	010
		12 x 10	011
		13 x 9	100
		14 x 8	101
	8M x 8	12 x 11	011
		13 x 10	100
		14 x 9	101
	16M x 4	12 x 12	011
		13 x 11	100
		14 x 10	101
256 Mbit	16M x 16	15 x 9	110
	32M x 8	15 x 10	110

Note: DRAC must be set to the same value as DRAC in the SA-1110.

Note that DRAC = 000 (for 9-bit Row Address) is not supported by the SA-1111, although a user could load that value into the register. If DRAC = 000 is loaded into the register, the controller will default to a 14-bit row address type (although the register will still read “000” for those bits). SDRAMs with 9-bit row address are an obsolete variety that is no longer available. The SA-1110, however, still supports that variation.

1.3.3 CAS Latency (Register SMCR, Bit 5 – CLAT)

The term “CAS Latency” specifies, for a read access, the number of clock periods from SDCAS/Read command assertion to valid read data out. CLAT corresponds to a value that is loaded into SDRAMs by the SA-1110 after power up, as part of system initialization. It tells the SDRAM how many cycles to wait (CAS latency) before enabling valid read data onto its data pins.

Note: CLAT on the SA-1111 must be set to the same value as CLAT in the SA-1110.

The SA-1111 normally runs SDRAMs at 48 MHz clock rate, typically much slower than the SA-1110 runs the SDRAMS. Theoretically, at this slow rate, read data is available internal to the SDRAMs at an earlier time, and a lower CAS latency could be used. However, the SDRAMs have been initialized to drive read data onto the bus during a specific clock cycle - a CAS latency time specified by CLAT written into the SA-1110 memory controller register. Regardless of its clock frequency, the SA-1111 memory controller must sample valid read data during the specified cycle, measured in integer clock cycles.

Support, Products, and Documentation

If you need general information or support, call **1-800-628-8686** or visit Intel's website at:

http://www.intel.com

Copies of documents that have an ordering number and are referenced in this document, a product catalog, or other Intel literature may be obtained by calling **1-800-548-4725** or by visiting Intel's website for developers at:

http://developer.intel.com