Bandwidth Calculations for SA-1110 Processor LCD Displays

Application Note

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Application Note

Contents

Figures

Tables

1.0 Introduction

This document describes the process for calculating the required data transfer rate to an LCD display by the Intel® StrongARM® SA-1110 microprocessor (SA-1110), which functions as the LCD controller, and the system timing considerations required to avoid display artifacts caused by memory bandwidth contention.

This application note should be used in conjunction with the *Intel® StrongARM® SA-1110 Microprocessor Technical Reference Manual*, Order Number 278240.

1.1 LCD Refresh Bus Bandwidth

The LCD refresh bus bandwidth calculations determines the amount of time required on the bus by the LCD controller to support an LCD panel, and helps identify bus timing that results in LCD screen artifacts caused by DMA starvation. To ensure the flicker-free operation of the LCD the system designer must consider the attributes of the LCD used, CPU speed, SDRAM, DRAM, Flash, ROM, and PCMCIA timing. For the purposes of this application note the processor core frequency is assumed to be 200 MHz.

The LCD memory bandwidth calculations are used with the following considerations:

- The LCD controller's DMA engine generates a relatively steady stream of 4-beat bus read transactions from memory (presumably SDRAM) to populate the on-chip palette and the LCD input FIFO. Because the relative speed of the memory where the LCD frame buffer is located has an impact on the bus bandwidth available for other system tasks, careful tuning of the on-chip memory controller will improve bus availability.
- While the LCD controller's DMA engine has the highest priority when requesting access to the bus, it must potentially share the bus with a variety of memory and hardware accesses performing 1- to 8-beat memory transfers. Memory devices that have long memory cycle times and perform repetitive accesses may cause perceptible screen flicker due to LCD DMA access delay.
- The system designer must also take into consideration bus overhead resulting from SDRAM refresh activity. The SDRAM refresh time should be included in the LCD bus bandwidth calculations as part of the fixed overhead to be deducted from the total bus bandwidth available to all other memory devices.

2.0 System Organization

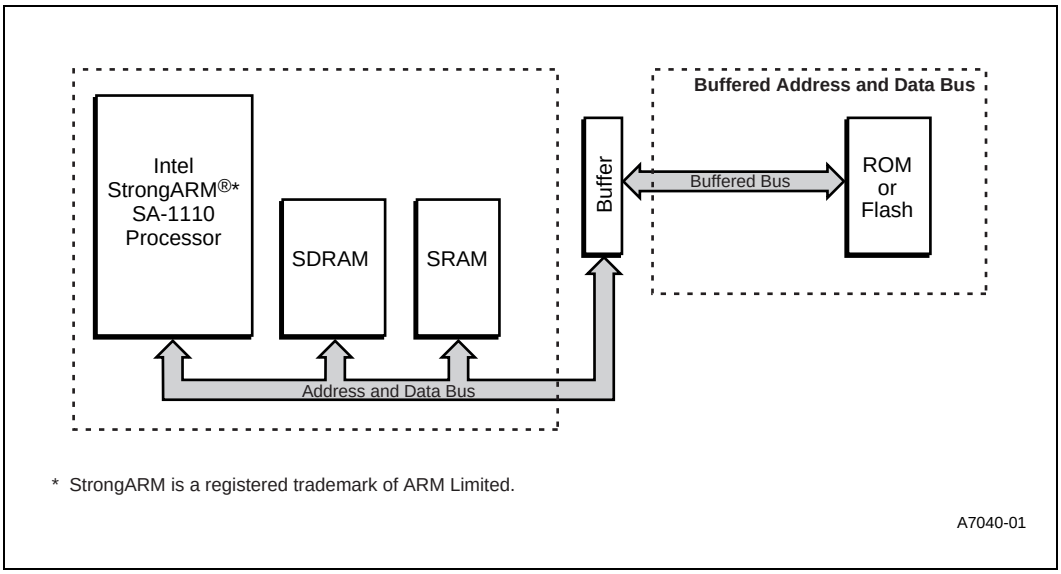
Both the type of memory and the placement of memory affects the memory bandwidth for SA-1110 designs. Many different types of memory can be used, each with different access times:

- SDRAM—typically 50 ns access time, 10 ns SDCLK burst cycle time.
- DRAM—typically 50 ns access time, 20 ns CAS burst cycle time.
- SRAM—typically 5 ns to 80 ns access time.
- ROM/Flash—typically up to 150 ns access time.

The SA-1110 processor typically supports up to four component loads (2 mA Ioh and Iol into 50 pF). For additional input/output support, signal fan-out buffers and transceivers must be used to connect address, control, and data signals to the SA-1110. These devices add approximately 10 ns of round-trip delay to CPU memory read operations.

Figure 1 shows an efficient system organization with the address and data bus providing immediate access to the fastest memory components—the SDRAM and SRAM. The buffered address and data bus does incur approximately 10ns of delay to the slowest memory components (Flash memory, ROM, and PCMCIA.)

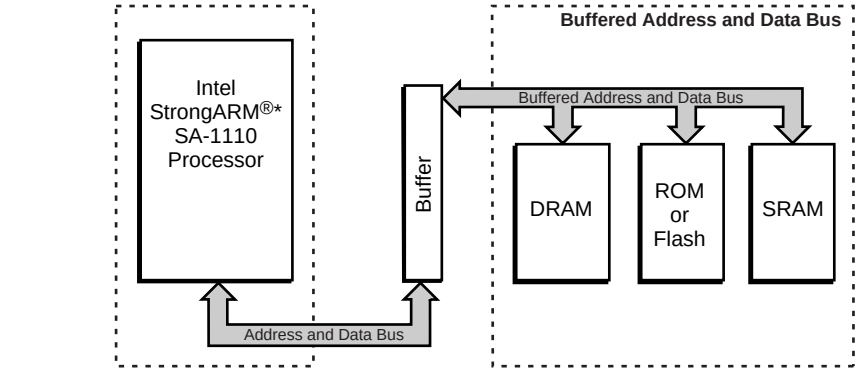
Figure 1. Efficient System Memory Organization



2.1 Less Efficient System Organization

Figure 2 shows a less efficient system organization with access to all of the memory components through a buffer. The buffer adds an additional 10 ns of round-trip delay that increases the access time to the SRAM, DRAM, ROM/Flash memories and PCMCIA.

Figure 2. Inefficient System Memory Organization



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3.0 Required LCD Data Rates for Display Refresh

Table 1 shows the data rates required to support a variety of typical display sizes and pixel depths at an arbitrarily selected refresh rate of 60 Hz. Note as the refresh rate increases, a larger proportion of the total available bus bandwidth is consumed by the LCD controller. The LCD data rates were calculated using the following formula:

$$\frac{\text{length} \times \text{width} \times \text{bits per pixel} \times \text{refresh rate}}{8 \text{ (for bytes)}}$$

Note: Because 12 bits are stored in memory as 16 bits, the bandwidth for 12 bits and 16 bits is the same. The data required to load the LCD controller palette (either 32 or 512 bytes per frame) is omitted from this calculation, as is non-displayed data required by some LCD panels for proper operation.

Table 1. LCD Data Requirements with 60 Hz Refresh (Sheet 1 of 2)

Length × Width	Bit per Pixel	Data Rate Required
1024 × 1024	1	7.864 MBytes/Second
1024 × 1024	2	15.728 MBytes/Second
1024 × 1024	4	31.457 MBytes/Second

Table 1. LCD Data Requirements with 60 Hz Refresh (Sheet 2 of 2)

Length × Width	Bit per Pixel	Data Rate Required
1024 × 1024	8	62.914 MBytes/Second
1024 × 1024	12	125.829 MBytes/Second
1024 × 1024	16	125.829 MBytes/Second
1024 × 768	1	5.898 MBytes/Second
1024 × 768	2	11.796 MBytes/Second
1024 × 768	4	23.592 MBytes/Second
1024 × 768	8	47.186 MBytes/Second
1024 × 768	12	94.372 MBytes/Second
1024 × 768	16	94.372 MBytes/Second
800 × 600	1	3.6 MBytes/Second
800 × 600	2	7.2 MBytes/Second
800 × 600	4	14.4 MBytes/Second
800 × 600	8	28.8 MBytes/Second
800 × 600	12	57.6 MBytes/Second
800 × 600	16	57.6 MBytes/Second
640 × 480	1	2.304 MBytes/Second
640 × 480	2	4.608 MBytes/Second
640 × 480	4	9.216 MBytes/Second
640 × 480	8	18.432 MBytes/Second
640 × 480	12	36.864 MBytes/Second
640 × 480	16	36.864 MBytes/Second
320 × 240	1	576 Kilobytes/Second
320 × 240	2	1.152 MBytes/Second
320 × 240	4	2.304 MBytes/Second
320 × 240	8	4.608 MBytes/Second
320 × 240	12	9.216 MBytes/Second
320 × 240	16	9.216 MBytes/Second

4.0 Calculating LCD Refresh Bus Bandwidth

The LCD bandwidth formulas below provide a means to determine if any given LCD and SA-1110 system configuration will function without visible video artifacts, and the amount of time the LCD refresh operation takes every second. The timing values obtained can be used to determine the maximum LCD refresh rate for any given LCD and SA-1110 system timing configuration, and the remaining system task memory bus bandwidth.

The first step is to determine the LCD data rate required to support the LCD panel selected for the system. The LCD data rate can be obtained from Table 1, or calculated using the formula shown in Section 3.0 above:

LCD byte count x frame rate = Mbytes/second

The next step is determining the number of 4-beat burst operations (4 bytes/beat) that are generated by the LCD DMA controller:

(Mbytes/second)/16 = LCD DMA burst count

The time consumed by the LCD refresh operation is then calculated:

LCD DMA burst count x Pdma = LCD refresh time/second

The value of Pdma is the period in microseconds of an LCD DMA four-beat burst, including DRAM or SDRAM precharge time. The time remaining within each second after the LCD refresh time is deducted is available for instruction and data fetches, hardware accesses, and memory refresh operations.

Note: The PCMCIA timing for the SA-1110 processor is reset to the longest possible cycle length upon power-up. The application should re-program the MECR register to adjust the PCMCIA cycle time appropriate to the system design requirements.

4.0.1 Bandwidth Calculations for Typical System Configurations

Table 2 shows the bandwidth available using various memory configurations and cache states when driving a 640 x 480 pixel LCD panel with a color depth of 8 bits, and a refresh rate of 60Hz, resulting in an LCD data rate of 18.432 Mbytes/second. The value Plcyc is the period in microseconds of program-driven memory access cycles, which can vary in length from one- to eight-beat bursts. Note that the program bandwidth shown below assumes maximum bus utilization without accounting for DRAM or SDRAM refresh cycles.

Table 2. Bandwidth with Typical Memory and Cache Configuration (Sheet 1 of 3)

Operation	Frame Buffer Memory Type	LCD Refresh Time (per second)	Program Location	Program Bus Time/Bandwidth
Executing from ROM with Cache disabled	DRAM (60 nS) with a Pdma of 0.25 µs (MDCAS00 = 0001 1000 1100 0110 0011 0001 1000 0111 MDCAS01 = 1100 0110 0011 0001 MDCNFG:TRP0 = 4 MDCNFG:CDB20 = 1 MDCNFG:TDL0 = 10)	288 milliseconds	Flash memory with a Plcyc of 0.16 µs (MSC0:RDF0 = 08 MSC0:RRR0 = 3)	712 milliseconds/ 17.8 MBytes/second

Table 2. Bandwidth with Typical Memory and Cache Configuration (Sheet 2 of 3)

Operation	Frame Buffer Memory Type	LCD Refresh Time (per second)	Program Location	Program Bus Time/Bandwidth
Executing from ROM with Cache disabled	SDRAM with Pdma of 0.10µs (MDCAS00 = 0101 0101 0101 0101 0101 0101 0101 0111 MDCAS01 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCAS02 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCNFG:DTIM0 = 1 MDCNFG:DWID0 = 0 MDCNFG:DRAC0 = 5 MDCNFG:CDB20 = 0 MDCNFG:TRP0 = 1 MDCNFG:TDL0 = 3)	115 milliseconds	Flash memory with a Plcyc of 0.16 µs (MSC0:RDF0 = 08 MSC0:RRR0 = 3)	885 milliseconds/ 22.1 MBytes/second
Executing from ROM with Cache enabled	DRAM (60 nS) with a Pdma of 0.25 µs (MDCAS00 = 0001 1000 1100 0110 0011 0001 1000 0111 MDCAS01 = 1100 0110 0011 0001 MDCNFG:TRP0 = 4 MDCNFG:CDB20 = 1 MDCNFG:TDL0 = 00)	288 milliseconds	Flash memory with a Plcyc of 0.86 µs (MSC0:RDF0 = 08 MSC0:RDN0 = 9 MSC0:RRR0 = 3)	712 milliseconds/ 26.5 MBytes/second
Executing from ROM with Cache enabled	SDRAM with Pdma of 0.10µs (MDCAS00 = 0101 0101 0101 0101 0101 0101 0101 0111 MDCAS01 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCAS02 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCNFG:DTIM0 = 1 MDCNFG:DWID0 = 0 MDCNFG:DRAC0 = 5 MDCNFG:CDB20 = 0 MDCNFG:TRP0 = 1 MDCNFG:TDL0 = 3)	115 milliseconds	Flash memory with a Plcyc of 0.86 µs (MSC0:RDF0 = 08 MSC0:RDN0 = 9 MSC0:RRR0 = 3)	885 milliseconds/ 32.9 MBytes/second
Execution from DRAM, Cache enabled	DRAM (50 nS) with a Pdma of 0.21 µs (MDCAS00 = 0110 0110 0110 0110 0110 0110 0110 0111 MDCAS01 = 0110 MDCNFG:TRP0 = 3 MDCNFG:CDB20 = 1 MDCNFG:TDL0 = 00)	241 milliseconds	DRAM (50 ns) with a Plcyc of 0.37 µs	759 milliseconds/ 65.6 MBytes/second

Table 2. Bandwidth with Typical Memory and Cache Configuration (Sheet 3 of 3)

Operation	Frame Buffer Memory Type	LCD Refresh Time (per second)	Program Location	Program Bus Time/Bandwidth
Execution from SDRAM, Cache enabled	SDRAM with Pdma of 0.10µs (MDCAS00 = 0101 0101 0101 0101 0101 0101 0101 0111 MDCAS01 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCAS02 = 0101 0101 0101 0101 0101 0101 0101 0101 MDCNFG:DTIM0 = 1 MDCNFG:DWID0 = 0 MDCNFG:DRAC0 = 5 MDCNFG:CDB20 = 0 MDCNFG:TRP0 = 1 MDCNFG:TDL0 = 3)	115 milliseconds	SDRAM with Pcyc of 0.14µs	885 milliseconds/ 202.3 MBytes/second

4.1 Example: Determining Available Task Memory Bandwidth

Determine the LCD bandwidth given the following display parameters:

- Pdma = 0.1µs (SDRAM)
- 8 bits per pixel (bpp)
- 640×480 screen
- 60Hz frame (or refresh) rate

Use the following procedure to determine the fixed LCD bandwidth overhead required to display an image:

1. Determine the display data requirements by multiplying length times width times bits per pixel. Using the above parameters, 640 × 480 × 8bpp = 2,457,600 bits. To determine the number of bytes, divide 2,457,600 by 8, which equals 307,200 bytes per frame. (This information is also shown in Table 1 for various display sizes.)
2. Multiply the number of bytes per frame (307,200) by 60Hz (the frame rate) to determine the total number of bytes per second required to refresh the LCD. In this example the result of the calculation is 18,432,000 bytes/second.
3. Divide 18,432,000 bytes/second by 16 (16 bytes per 4-beat burst generated by LCD controller DMA activity) to determine the number of bursts per second, in this example 1,152,000 bursts per second.
4. Determine the total time per second the LCD controller is active on the bus updating the display by multiplying Pdma (0.1µs, LCD DMA transaction time) by 1,152,000 (number of 4-beat bursts per second generated by the LCD controller.) In this example, the result is 115.2 milliseconds of time per second consumed by the LCD controller driving screen update data to the LCD panel, leaving the remaining 884.8 milliseconds per second available for data and instruction fetching, memory refresh activity, LCD frame store updates, and so on. This LCD time calculation provides a rough indication of the proportion of time allocated to the fixed overhead of a given LCD configuration.
5. To avoid the generation of on-screen display artifacts (“flicker”) caused by LCD DMA access delay, the system designer must also take into consideration the timing of the memory devices other than the DRAM or SDRAM. If the number of LCD DMA bursts in the example above (1,152,000 bursts per second) are divided into one second, an LCD burst occurs every 868ns. If ROM is being repetitively accessed through 8-beat bursts with a Plcyc equal to 1.0µs, the ROM memory cycle may cause the LCD DMA access to be delayed, and screen flicker may result. Note that this example does not take into account LCD frame and line delay timing, and assumes that the LCD DMA accesses are uniformly distributed throughout a given time period. Flicker-free display operation in systems with high bus utilization requires careful attention to size and depth of the display, the LCD frame rate, and balance in the use and speed of SDRAM, DRAM, SRAM, and ROM.

If the same LCD panel specified above was refreshed from a 50ns DRAM, the LCD controller bus access time per second calculation would proceed from step 4 above as follows:

- The total time per second the LCD controller is active on the bus is determined by multiplying the Pdma for the DRAM (0.21µs, LCD DMA transaction time) by 1,152,000 (number of 4-beat bursts per second.) The result is 242 milliseconds per second consumed by the LCD refresh task, leaving 758 milliseconds available for other system functions.

4.1.1 Error Interrupt Mask

To maximize bandwidth, the error interrupt mask should be set to one to block the generation of interrupt requests. The error interrupt mask is only enabled while developing software to determine when overflow and underflow events occur.

For more information on the error interrupt mask, see the *Intel® StrongARM® SA-1110 Microprocessor Advanced Developer's Manual*.

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