Bandwidth Calculations for SA-1100 Processor LCD Displays

Application Note

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Application Note

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1.0 Introduction

This document describes the process for calculating the bandwidth of data that can be transferred to the LCD display from a StrongARM™ SA-1100 device.

This application note should be used in conjunction with the following manuals:

- *SA-1100 Microprocessor Technical Reference Manual* (278088)
- *StrongARM™ SA-1100 Microprocessor Specification Update* (278105)

2.0 System Organization

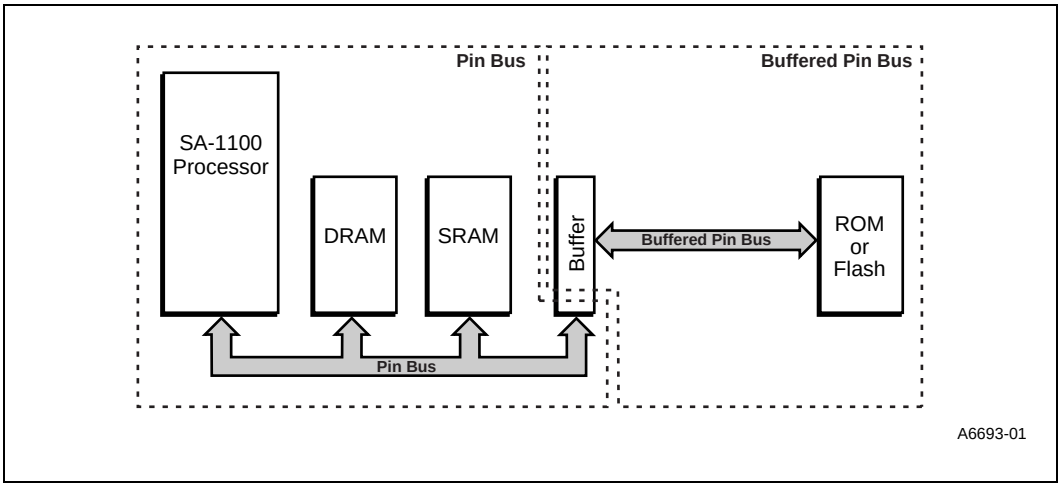
Both the type of memory and the placement of memory will drastically affect the memory bandwidth for the SA-1100 design. Many different types of memory can be used, each with different speeds:

- DRAM—typically 25ns CAS burst cycle time.
- SRAM—typically 5ns to 50ns access time.
- ROM Flash—typically up to 150ns access time.

The SA-1100 processor will typically support up to four component loads and three inches of etch. For additional input/output support, buffers must be used to disperse signals, which incur approximately 10ns of round-trip delay.

Figure 1 shows an efficient system organization with the pin bus providing immediate access to the fastest memory components—the DRAM and SRAM. The buffered pin bus does incur approximately 10ns of delay to the slowest memory components—the flash or ROM, but this delay only affects their access time by approximately 6%.

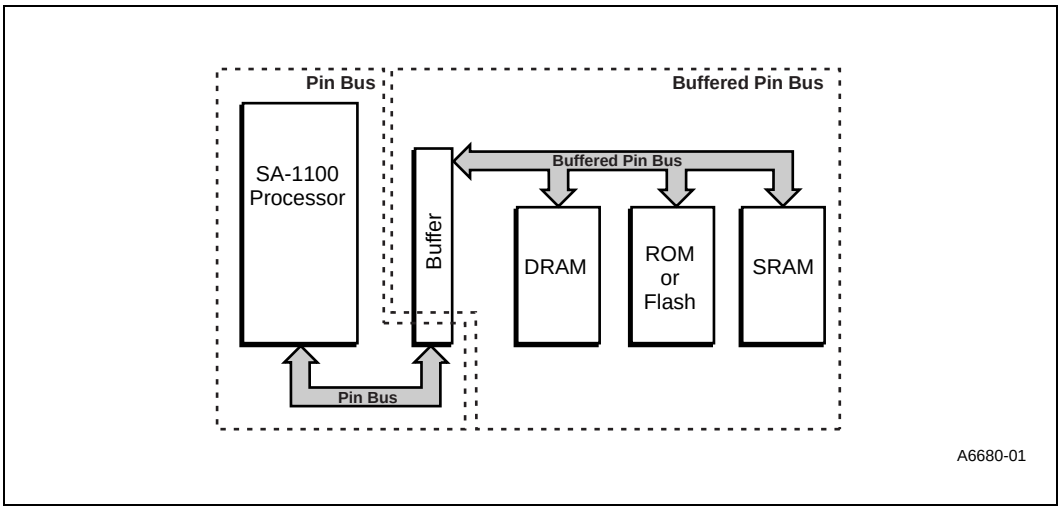
Figure 1. Efficient System Organization of Memory



2.1 Inefficient System Organization

Figure 2 shows an inefficient system organization with access to all of the components through the buffer. The buffer adds an additional 10ns of round-trip delay that increases the access time to the SRAM and DRAM by 50%.

Figure 2. Inefficient System Organization of Memory



3.0 Bandwidths for LCD Displays

Table 1 shows the range and bandwidth requirements for a variety of typical display sizes and pixel depths. These bandwidth requirements were calculated using the following formula:

$$\frac{\text{length} \times \text{width} \times \text{bits per pixel} \times \text{refresh rate} \times \text{blanking factor of 1.2}}{8 \text{ (for bytes)}}$$

Note: Because 12 bits are stored in memory as 16 bits, the bandwidth for 12 bits and 16 bits is the same.

Table 1. Bandwidth Requirements with 60 Hz Refresh (Sheet 1 of 2)

Length × Width	Bit per Pixel	Bandwidth Requirements
1024 × 1024	1	9.437 MB/s
1024 × 1024	2	18.874 MB/s
1024 × 1024	4	37.748 MB/s
1024 × 1024	8	75.497 MB/s
1024 × 1024	12	151 MB/s
1024 × 1024	16	151 MB/s
1024 × 768	1	7.077 MB/s
1024 × 768	2	14.155 MB/s
1024 × 768	4	28.311 MB/s

Table 1. Bandwidth Requirements with 60 Hz Refresh (Sheet 2 of 2)

Length × Width	Bit per Pixel	Bandwidth Requirements
1024 × 768	8	56.623 MB/s
1024 × 768	12	113 MB/s
1024 × 768	16	113 MB/s
800 × 600	1	4.32 MB/s
800 × 600	2	8.64 MB/s
800 × 600	4	17.28 MB/s
800 × 600	8	34.56 MB/s
800 × 600	12	69.12 MB/s
800 × 600	16	69.12 MB/s
640 × 480	1	2.764 MB/s
640 × 480	2	5.529 MB/s
640 × 480	4	11.059 MB/s
640 × 480	8	22.118 MB/s
640 × 480	12	44.236 MB/s
640 × 480	16	44.236 MB/s
320 × 240	1	691 KHz
320 × 240	2	1.382 MB/s
320 × 240	4	2.764 MB/s
320 × 240	8	5.529 MB/s
320 × 240	12	11.059 MB/s
320 × 240	16	11.059 MB/s

4.0 Calculating Maximum Bandwidth

The maximum LCD bandwidth calculation determines a sustainable LCD bandwidth without DMA starvation based upon a specific CPU speed, DRAM, flash, and PCMCIA timing.

This calculation is based on the following worst case situation:

- The LCD is running with a background of constant worst case long memory cycles (typically flash eight burst).
- The LCD DMA requests result in at least every other bus cycle being arbitrated in favor of the LCD such that the memory bus traffic is a continuous sequence of interleaved LCD DMA four bursts and flash eight bursts.

4.1 LCD Bandwidth Formula

The LCD bandwidth formula can be used to determine if any given LCD configuration and SA-1100 system timing will function without visible video artifacts. It can also be used to determine the maximum LCD refresh rate for any given LCD and SA-1100 system timing set.

The formula for calculating the maximum sustainable LCD bandwidth is:

LCDbw = 15/(Pdma+Plcyc)

Where:

- LCDbw is the number of megabytes per second (MB/s) of sustainable LCD bandwidth.
- 15 is the number of bytes in a four-cycle burst minus one. The minus one accounts for DRAM refresh overhead.
- Pdma is the period in microseconds of a LCD DMA DRAM four word burst, including precharge time.
- Plcyc is the period in microseconds of the longest bus cycle, which typically is a burst of eight from flash or ROM including precharge time, or a PCMCIA cycle.

Note: The PCMCIA timing for the SA-1100 processor is reset to the longest possible cycle length upon power-up. The application should re-program the MECR register to adjust the PCMCIA cycle time appropriate to the system design requirements.

4.1.1 Bandwidth Calculations for Typical System Parameters

The type of instruction execution and the type of memory will drastically affect bandwidth as shown in Table 2.

Table 2. Bandwidth with Different Hardware and Software

Operation	Pdma	Plcyc	Bytes/Second
Execute in Place (XIP) with Cache enabled[1]	Slow DRAM (60 nS) with a Pdma of 0.25 µs	Standard ROM (120 ns) with a Plcyc of 1.0 µs	12 MB/s
Execute in Place (XIP) with Cache disabled	Slow DRAM (60 nS) with a Pdma of 0.25 µs	Standard ROM (120 ns) with a Plcyc of 0.22 µs	32 MB/s
XIP	Fast DRAM (50 nS) with a Pdma of 0.15 µs	Page mode ROM[2] (25 ns) with a Plcyc of 0.4 µs	27.272 MB/s
Execution from DRAM only	Fast DRAM (50 nS) with a Pdma of 0.15 µs	Fast DRAM (50 ns) with a Plcyc of 0.235 µs	38.961 MB/s

1. Enabling the cache increases the Plcyc parameter by up to eight times.
2. Using Intel's 3 Volt Fast Boot Block Flash memory device (28160K3) with the SA-1100 programmed for burst ROM reads (page mode flash).

4.2 Example 1: Calculated Maximum Screen Refresh Rate for 640×480 Screen, 8bpp

Determine the maximum sustainable bandwidth with the following parameters:

- Pdma = 0.3µs (20ns DRAM)
- Plcyc = 1.0µs
- 8 bits per pixel (bpp)
- 640×480 screen

Use the following procedure to determine the highest possible screen refresh rate:

1. Determine the display requirements by multiplying length times width. Using the above parameters, 640 × 480 × 8bpp = 2,457,600. To determine the number of bytes, divide 2,457,600 by 8, which equals 307,200 bytes. Consider a blanking factor of 1.2, which is about 20% and typically ranges from 10% to 25%. This results in 307,200 × 1.2 = 368,640, which is the effective bytes per screen.
2. Calculate the period of Pdma plus Plcyc, which is.3 µs plus 1.0 µs, for a total of 1.3 µs. The frequency is the reciprocal of 1.3 µs, which is 769,230 Hz for 1/15 of the bytes.
3. Multiply 15 times the frequency, which results in 11,538,461 bytes per second or about 11.5 MB/s. The maximum sustainable bandwidth is 11.5 MB/s from the 20 ns DRAM while not executing XIP instructions.
4. Calculate the maximum screen refresh rate by dividing the maximum sustainable bandwidth by the effective bytes per screen. This results in 11.5 MB/s divided by 368,640 that equals 31.3 Hz. The maximum screen refresh rate using these system parameters is 31.3 Hz.

4.2.1 Error Interrupt Mask

To maximize bandwidth, the error interrupt mask should be set to a one to block the generation of interrupt requests. The error interrupt mask is only enabled while developing software to determine overflow and underflow operations.

For more information on the error interrupt mask, see the *StrongARM™ SA-1100 Microprocessor Technical Reference Manual*.

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