ARM 7500FE

Data Sheet

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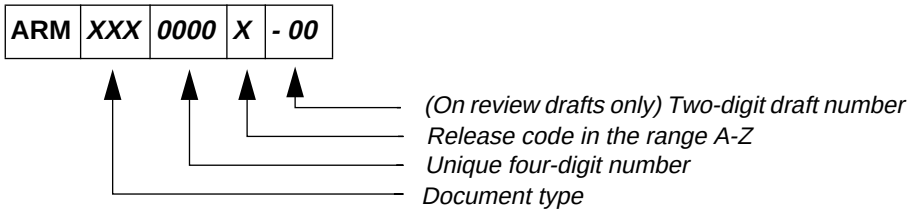

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Change Log

Issue	Date	By	Change
A	Aug 1996	SKW	Released as preliminary version
B-01	Sep 1996	SKW	Amendments and update to general release

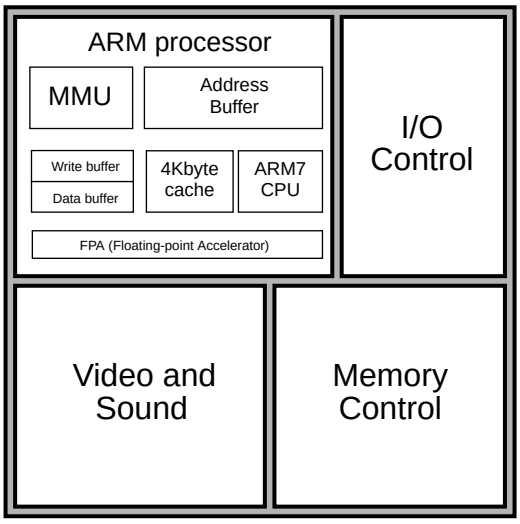
Preface

ARM7500FE is a highly integrated, multi-media single-chip computer, based around the ARM RISC microprocessor macrocell. ARM7500FE contains all the functionality required to create a complete computing system with the minimum of external components.The wide range of features incorporated into ARM7500FE makes it an extremely flexible device, which can be programmed according to the required application to optimise for high performance or low power, or a combination of both.

Features

- Highly integrated RISC computer
- 36.3 Dhrystone 2.1 MIPS ARM7 core @ 40MHz CPU clock
- 5.7 million SAXPY loops, or up to 6 double-precision Linpack MFLOPS (at 40MHz)
- 4 Kbyte combined instruction and data cache
- Flexible Memory Management Unit
- Glueless memory interface (16 or 32 bits wide) for ROM, RAM and EDO DRAM
- 128 MBytes/sec (peak) memory bandwidth using 64MHz memory clock
- 3 channel DMA controller (for video, cursor and sound data)
- I/O controller, including PC-style bus
- 2 serial ports, 4 A/D channels
- 32-bit CD quality serial sound channel
- Video controller with up to 120MHz pixel clock; resolutions up to 1024 x 768 pixels
- 16 million colours from 256-entry palette, and 16-level grey scales for LCD displays
- Direct RGB drive of CRTs; support for interlaced TV displays
- Suspend and stop power-saving modes

Block diagram of the ARM7500FE

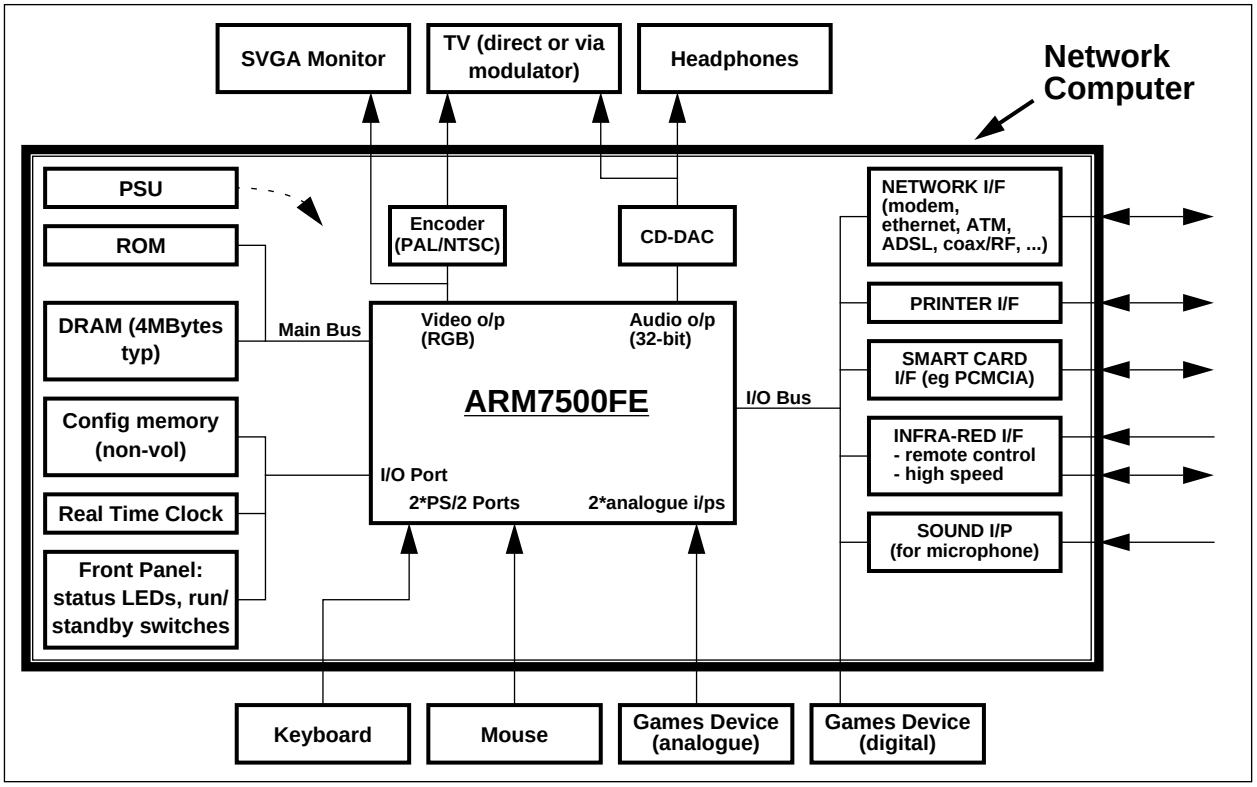


Applications

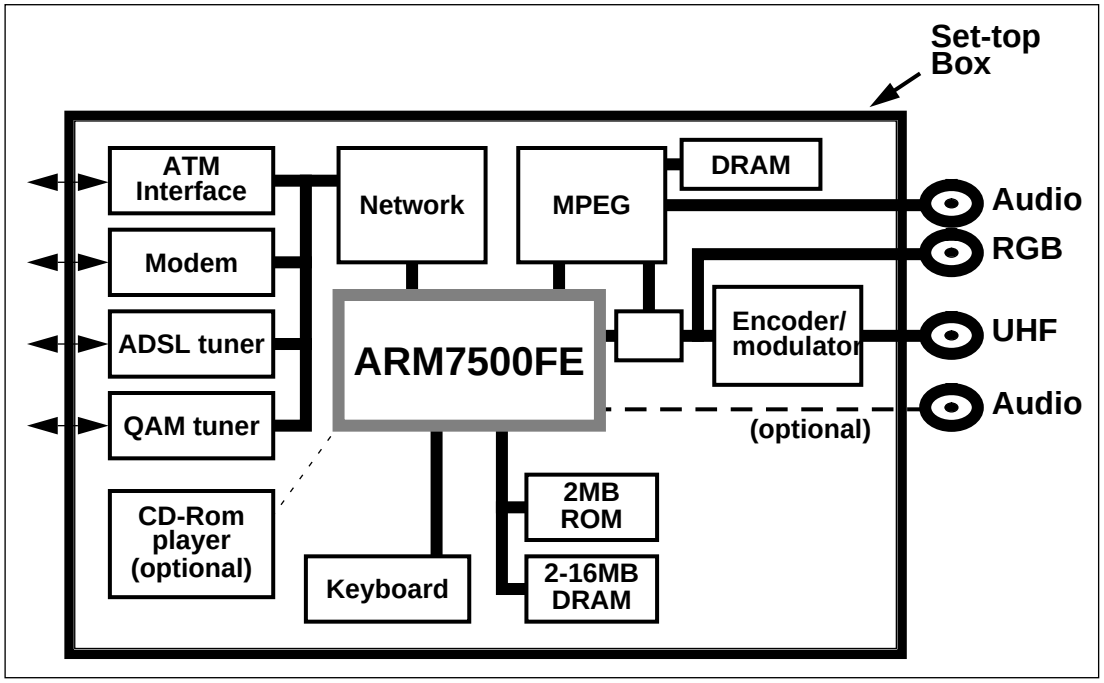
ARM7500FE is ideally suited to applications requiring a compact, low-cost, power-efficient, high-performance, RISC computing system on a single chip. These include:

Multimedia	Internet appliances and set-top boxes (see page iv)
Portable Computing	Handheld test instrumentation
Games consoles	Desktop computing

Application Example 1: Network Computer



Application Example 2: Set-top Box for Digital Interactive Television



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Datasheet Notation

0x	marks a Hexadecimal quantity
BOLD	external signals are shown in bold capital letters
binary	where it is not clear that a quantity is binary it is followed by the word binary

Preface

Contents

1 Introduction

This chapter introduces the ARM7500FE single-chip microprocessor.

Introduction

1.1 Introduction

ARM7500FE is a high-performance, low-power RISC-based single-chip computer centered around the ARM microprocessor core. To maximize the potential of the ARM processor macrocell, ARM7500FE contains memory and I/O control on-chip, enabling the direct connection of external memory devices and peripherals with the minimum of external components. A floating-point accelerator (FPA) is also integrated, resulting in outstanding maths performance.

ARM7500FE includes features which also make it particularly suitable for low-power portable applications. Both 32 and 16-bit wide memory systems are supported, allowing a lower-cost 16-bit-based system to be designed. The ARM7500FE will drive color CRT or color LCD panels. Monochrome single or dual panel LCDs with 16 levels of greyscaling can also be driven. Power-management circuitry is included with two power-saving states. The high level of integration achieved allows significant PCB area saving, and results in a very cost-competitive system.

ARM7500FE is also particularly suited to any application requiring high-quality video, sound and general I/O requirements, such as multimedia. The video controller provides up to 16 million colors from a 256-entry palette, running at up to 120MHz pixel clock rate. The sound subsystem includes a serial sound interface for CD quality 32-bit sound. Four on-chip A to D converters allow the connection of analog joysticks or similar control devices. The clocking scheme is very flexible, allowing either a very cheap system to be built using a single oscillator, or separate asynchronous clocks to be used for the CPU, memory and I/O subsystems, which gives an extremely flexible system, able to take advantage of the fastest available DRAM memory.

The wide range of features incorporated into ARM7500FE make it an extremely flexible device, which can be programmed according to the required application to optimise for high performance or low power, or a combination of both.

1.2 Functional Block Diagram

Figure 1-1: Block diagram of the ARM7500FE on page 1-3 gives a more detailed view of the functionality of the ARM7500FE single-chip computer.

1.3 ARM Processor Macrocell

The ARM processor contains an ARM7 core with MMU, 4K cache, and write buffer.

1.4 FPA Macrocell

The FPA is a fully IEEE-754 compliant floating-point accelerator, and supports single, double and extended precision formats. It is connected to the ARM via the coprocessor interface and provides the same floating-point functionality as the FPA11.

Concurrent load/store and arithmetic units, and speculative execution are employed to give good floating-point performance.

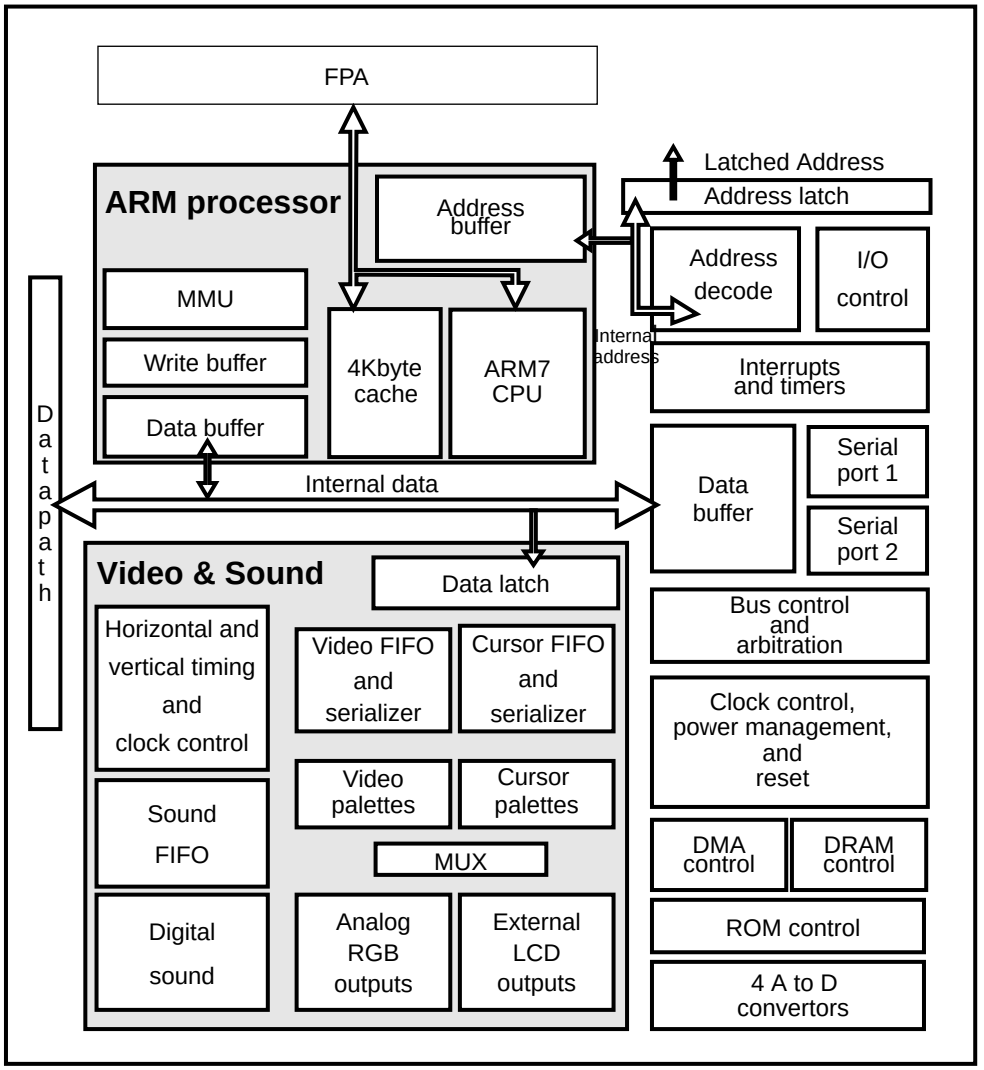

Figure 1-1: Block diagram of the ARM7500FE

1.5 Video and Sound Macrocell

The video and sound macrocell gives the ARM7500FE the flexibility to drive high specification CRT or low power LCD displays, and features the following:

- up to 120MHz pixel clock rate
- resolutions of up to 1024 x 768 pixels are directly supported (greater if external serialization is used)
- fully programmable display parameters
- 256-entry by 28 bit video palette
- red, green and blue 8-bit linear DACs to drive CRT
- 1,2,4,8,16,32 bits/pixel CRT modes
- up to 16 million colors
- external bits in palette for supremacy, fading, Hi_Res
- single or dual panel LCD driving
- 16-level grey scaler for LCD
- power-management features
- hardware cursor for all display modes
- sound system — serial CD digital output

1.6 Clock Control and Power Management

The clocking strategy for ARM7500FE has been designed for maximum flexibility, and includes separate clock inputs for the:

- CPU core clock
- Memory system clock
- I/O system clock (in addition to the video clock inputs).

Each of the three clock inputs has a selectable divide-by-two prescaler to generate an internal 50/50 mark-space ratio if required. Throughout this datasheet, all timing diagrams assume that **CPUCLK**, **MEMCLK**, and **I_OCLK** are divided by one.

There are two levels of power management included.

SUSPEND mode	The clock to the CPU is stopped, but the display continues to work normally, ie. DMA unaffected.
STOP mode	All clocks are stopped. Two asynchronous wake-up event pins are provided to terminate stop mode. Circuitry is included on chip to stop external oscillators and restart them cleanly when required.

1.7 Memory System

The memory system interface control logic is completely asynchronous in operation to the I/O control logic. This means that the clock to the memory controller can be increased in frequency to allow faster memory to be used. This implementation gives maximum system flexibility.

ARM7500FE can control a 32 or 16-bit wide memory system. The width of each bank of ROM or DRAM is selectable by programming appropriate register bits. Fast Page Mode or EDO DRAM types are supported.

A DRAM controller is included which can directly drive up to 4 banks of DRAM. Four **nRAS** strobes individually select one of the four banks, and four **nCAS** strobes provide individual byte selection. The DRAM address multiplexing option provided allows a wide variety of DRAM sizes from 256K to beyond 16MB to be used. Up to 256 page mode transfers may occur in one sequential burst. When configured for operation with a 16-bit DRAM system, the DRAM controller will convert the access into two DRAM cycles to access the two halves of the 32-bit word. Byte transfers will only take one DRAM access cycle, even in 16-bit mode.

A programmable register allows one of four DRAM refresh rates to be selected. In addition, a register is provided to enable direct software control of the **nCAS** and **nRAS** lines for setting DRAM into a self-refresh state.

A ROM controller supports two 16MB banks of ROM with individually programmable read cycle timings. Support is provided for burst mode reads. Each ROM bank can be programmed to operate in 16-bit wide mode, and like the DRAM controller will convert accesses into two ROM cycles for the two halves of the 32-bit word. The ROM controller can be programmed to allow write cycles through this interface, allowing FLASH to be programmed, for example.

1.7.1 DMA

Three fully programmable DMA channels are included, for video, cursor and sound data. The DMA controller includes additional support for dual panel LCDs.

1.7.2 I/O control

The I/O bus of ARM7500FE is 16-bits wide but for some types of access can be expanded to 32 bits by the use of external transceivers. The input clock I_OCLK provides a reference for the I/O subsystem which is nominally 32MHz. The I/O features of this device can be separated into 3 distinct cycle types:

- Simple I/O with fixed 8MHz timings
- Module I/O with variable length 8MHz timings
- PC bus style I/O with fixed 16MHz timings and support for 32-bit data

Simple I/O

The Simple I/O type of access is 16-bit only and has a selection of 4 different cycle speeds selectable by address. When writing, the upper half-word of the ARM data bus is written out on the I/O bus. When reading, the I/O bus data is read back onto the lower half-word of the ARM data bus. During these accesses, a chip select is asserted with the appropriate **nIOR**/**nIOW** read or write strobe, based on the 8MHz clock **CLK8**.

Module I/O

The Module I/O type of access is 16 bit only and its timing is controlled by a handshake mechanism with the external hardware. The signals **nIORQ** (output) and **nIOGT** (input) are used for this handshaking and are referenced to **REF8M**. When writing, the upper half-word of the ARM data bus is written out on the I/O bus. When reading, the I/O bus data is read back onto the lower half-word of the ARM data bus.

During these accesses, a chip select is asserted but the **nIOR**/**nIOW** read and write strobes are not used, although the **IORNW** signal is active.

PC bus style I/O

The PC bus style I/O type of access routes the lower half-word of the ARM bus through the device providing a direct 16-bit interface. Signals are generated to support the addition of external latches/drivers to extend the I/O data by 16 bits. The upper half-word of the ARM data bus is routed through these external devices if present.

There are 5 different address areas generating 5 different chip selects using the same type of access. There are 4 fixed cycle types based on the 16MHz clock, although the largest area only supports two of these cycle types. Any access may be held up by external circuitry removing the **READY** signal before the end of the cycle.

During these accesses, the relevant chip select is asserted as well as read or write strobes as appropriate.

Two special inputs are provided to allow external circuitry to route the full 32 bits through the 16-bit I/O bus using multiplexing. This would allow, for example, the execution of code from a 16-bit PCMCIA card with suitable external controller. On a read I/O, if this latching signal is used, the data read back onto the ARM data bus comes from the I/O bus instead of the external extension latches.

1.8 Other Features

ARM7500FE includes four analog comparators, which can be used to create four A to D converter channels, and two serial keyboard/mouse ports.

There are 8 general-purpose open-drain I/O lines which can be used as inputs or open drain outputs and as interrupt sources if required.

An interrupt handler processes a variety of internal and external interrupt sources to generate the IRQ and FIQ interrupts for the ARM processor.

1.9 Test Modes

ARM7500FE has an **nTEST** pin which is used to invoke various test modes. When **nTEST** is set LOW, the functionality of many of the pins will change depending on the values applied to the **nINT3**, **nINT6** and **nINT8** pins. The **nTEST** pin includes an on-chip pull-up, but it is recommended that the pin be pulled up to VDD externally too. See *Appendix F: ARM7500FE Test Modes*.

Note: *The **nTEST** pin should never be forced LOW during normal operation.*

1.10 Structure of ARM7500FE

ARM7500FE includes three modified ARM macrocells:

- the ARM processor
- the FPA
- the video/sound macrocells

These macrocells are self-contained and the relevant control registers are contained within them. This has the effect that there are four sets of programmable registers within the ARM7500FE, which are accessed in different ways depending on their location.

1.10.1 Register programming

The ARM processor register programming is described in *Chapter 4: The ARM Processor Programmers' Model* .

The FPA register programming is described in *Chapter 9: Floating-Point Coprocessor Programmer's Model* .

The video and sound macrocell's registers are programmed using only the internal ARM7500FE data bus (the address bus is not passed to the macrocell). The address 0x03400000 is decoded to provide a write strobe for the video macrocell registers, and the addressing of registers within the macrocell is decoded from the upper four or eight bits of the data word. This system is described more fully in *Chapter 12: The Video and Sound Programmer's Model* .

The remaining ARM7500FE registers, associated with Memory, I/O and general miscellaneous control, form a separate group and are programmed between addresses 0x03200000 and 0x032001F8. The majority of the registers are only eight bits wide, although all register addresses are word-aligned. These registers are described in *Chapter 16: Memory and I/O Programmers' Model* .

1.10.2 Interaction between macrocells

Interaction between the macrocells occurs mainly across the ARM7500FE's internal 32-bit data bus, which is routed to the ARM and video/sound macrocells, and most of the other memory and I/O control logic. The ARM processor's address bus is routed to an internal address decoder where memory space is decoded to determine required cycle types and register addresses. The same address bus is latched and exported from the chip as the **LA[28:0]** bus. Only these 29 bits of the address bus are available externally.

1.11 Resetting ARM7500FE Systems

The ARM7500FE is designed to operate with both 16 and 32-bit wide ROM, which means that it must be capable of booting from either. To achieve this, the chip is always reset into 16-bit mode, which might be expected to cause difficulty when the chip is being booted up from 32-bit ROM. However, *Appendix A: Initialization and Boot Sequence* describes a simple code sequence which will allow the chip to be started up without difficulty under these circumstances.